# DAB One-Chip Channel- and Source Decoder

## Description

The U2739M-B is an integrated circuit in advanced CMOS technology for demodulation and decoding of a DAB signal according to ETS 300 401. The channel decoder part includes the main features OFDM demodulation & decoding and time & frequency synchronization algorithms, using the embedded OAK DSP core.

The source decoder consists of an audio and a data decoder part. The audio source decoder supports ISO MPEG 1,2 layer 2 and the data decoder offers 2 independent packet mode decoders.

Several standard interfaces, like $I^2C$/L3, $I^2S$, SPDIF or RDI are implemented to offer a flexible utilization.

Moreover the U2739M-B includes a mechanism to replace respectively extend certain software modules by using a special boot mode (so-called USE). For example, the time & frequency synchronization modules can be replaced by down-loading the corresponding user software algorithms to the OAK DSP core.

Electrostatic sensitive device.
Observe precautions for handling.

## Block Diagram

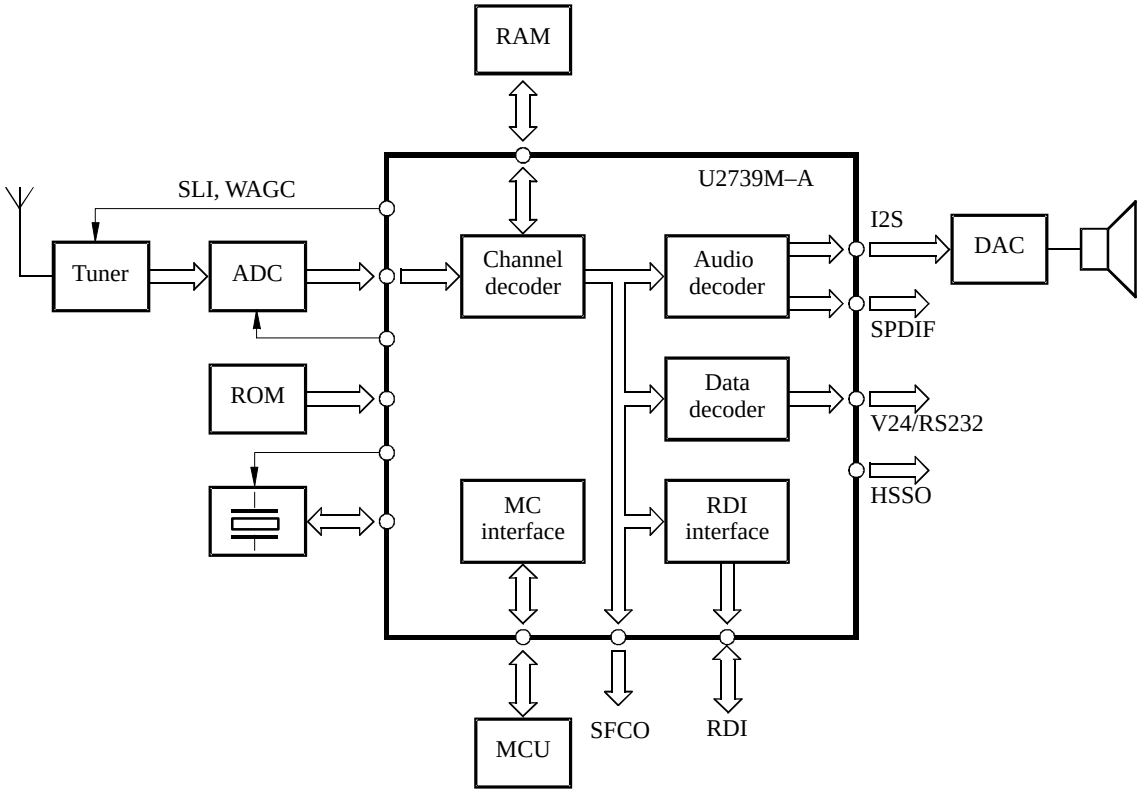



Figure 1. Block diagram

## Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U2739M-BFT | T–PQFP–G100 | Tray |
| U2739M-BFC | CQFP144 | Tray |

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# 1 Features

## 1.1 General

- Support of mode I, II, III and IV acc. to ETS 300 401
- Time & frequency synchronization with a wide-range parameter set
- Optional implementation of user-defined synchronization strategy by using USE boot mode
- Flexible software configuration:
  set 1 – (temic kernel), set 2 – (user extension) concept
- Automatic mode detection (AMD)
- FIC on-chip memory, access via MC interface
- Generation of receiver status information
- Generation of tuner control signals
- Generation of pulse width modulated VCXO control signal
- Power supply 3.3 V, master clock 24.576 MHz
- Plastic TQFP100 package or
- Ceramic QFP144 package for software development

## 1.2 Channel Decoder

- Demodulation and decoding of up to 64 UEP/EEP sub-channels
- Support of dynamic multiplex reconfiguration (DMR) without mute state
- Digital Null-Symbol detection (FSYNCH generation)
- Channel filtering (48 dB)
- Optional SAW filter equalization
- Digital AFC (freq. tolerance < 0.5 Hz for mode I)
- Digital AGC with a wide gain control range
- Off-chip de-interleaver memory for full 1.8 Mbit/s decoding data rate
- Time & frequency synchronization on DSP OAK core
- Support of TII decoding and corresponding RDI insertion (set 2)

## 1.3 Audio Source Decoder

- Supports MPEG1 layer II streams according to ISO/IEC 11172/3
- Supports MPEG2 layer II (half sampling rate) streams according to ISO/IEC 13818–3
- Supports all bit rates defined in the ETS 300 401 standard
- $I^2S$ and SPDIF output interfaces
- Programmable fader
- Programmable DRC
- PAD extraction

## 1.4 Data Decoder

- 2 independent packet mode decoder
- Flexible configuration via MC commands
- Data group length limited to ~1 kbyte each
- Output via HSSO or V24
- DD1 option: FIDC decoder
- Support of AIC decoding (set 2)

## 1.5 Interfaces

- Source decoder output interface: $I^2S$ and SPDIF
- Data decoder output interface: V24 or HSSO
- Channel decoder output interface: RDI and SFCO
- Microcontroller interface: $I^2C$/L3
- RDI:
  - Extended high capacity mode
  - IEC 958 format
  - RDI control channel (RCC)
- SFCO simple full capacity output:
  - window-, serial sub-channel identifier (SbChId)-, data-, error- and clock line
  - 3.072 MHz burst mode interface
- 10-bit ADC interface:
  - ADC sampling clock generation
  - ADC binary or 2's complement format selection
  - support of several intermediate frequencies
- DSP OAK core bootstrap ROM interface
- Voltage controlled reference oscillator (VCXO) interface
- Time de-interleaver SRAM (4 Mbit) interface
- High speed serial output HSSO (PAD, DD1, DD2, CIR) interface, 3-line serial burst mode interface

# 2 Functional Block Diagram

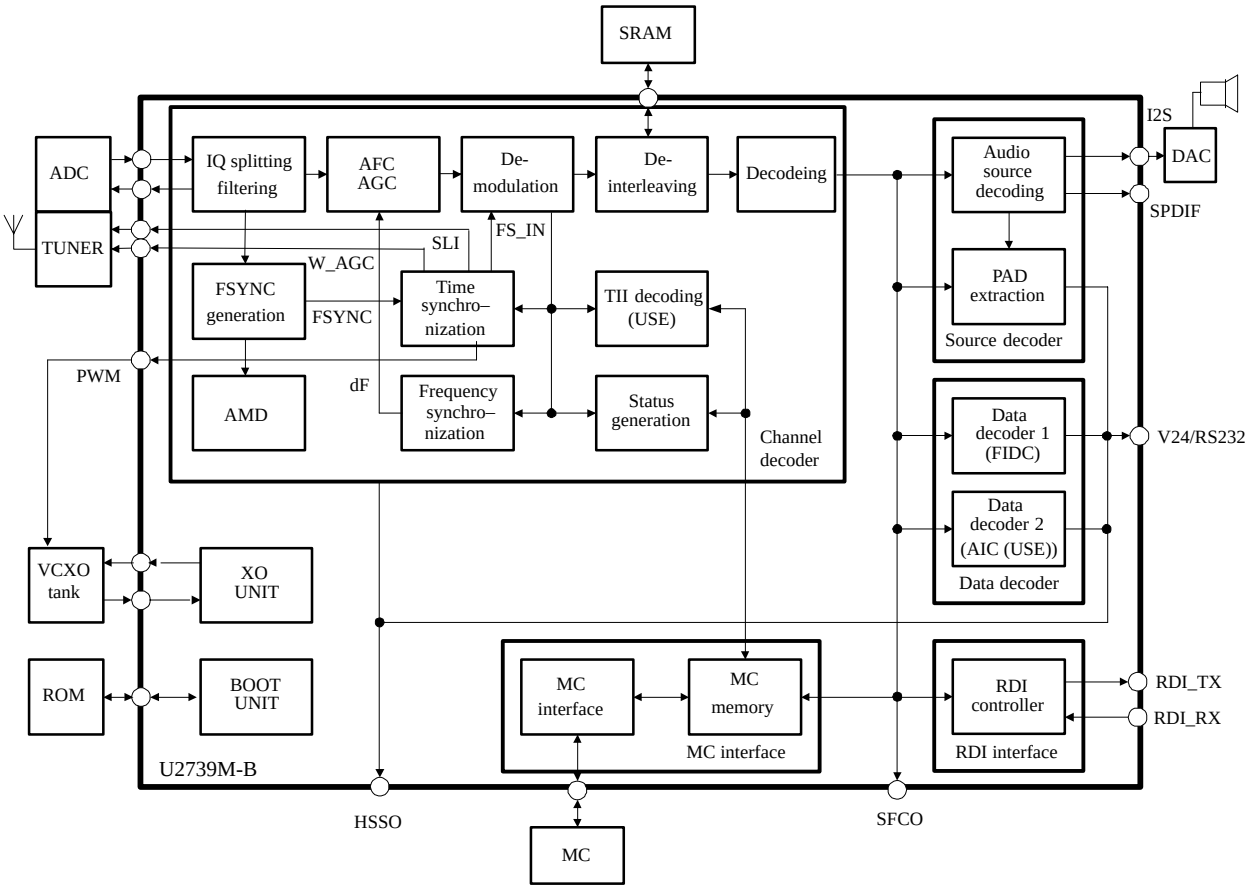



Figure 2. Functional block diagram

# 3 Pin Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 1 | 1 | ADC_CLK | ADC sampling clock output 8.192 MHz | PDO04T | out | |
| 2 | | TIN0 | Test input 0 (pull down) | PDDZ | in | x |
| 3 | | TIN1 | Test input 1 (pull down) | PDDZ | in | x |
| 4 | 2 | ADC_DATA9 | ADC data input, bit 9 (MSB) | PDIZ | in | x |
| 5 | 3 | ADC_DATA8 | ADC data input, bit 8 | PDIZ | in | x |
| 6 | 4 | ADC_DATA7 | ADC data input, bit 7 | PDIZ | in | x |
| 7 | 5 | ADC_DATA6 | ADC data input, bit 6 | PDIZ | in | x |
| 8 | | TIN2 | Test input 2 (pull down) | PDDZ | in | x |
| 9 | | DVSSE | Ground | PVSS1Z, PVSS2Z | gnd | x |
| 10 | 6 | ADC_DATA5 | ADC data input, bit 5 | PDIZ | in | x |
| 11 | 7 | ADC_DATA4 | ADC data input, bit 4 | PDIZ | in | x |
| 12 | 8 | ADC_DATA3 | ADC data input, bit 3 | PDIZ | in | x |
| 13 | 9 | ADC_DATA2 | ADC data input, bit 2 | PDIZ | in | x |
| 14 | | TIN3 | Test input 3 (pull down) | PDDZ | in | x |
| 15 | | TIN4 | Test input 4 (pull down) | PDDZ | in | x |
| 16 | 10 | ADC_DATA1 | ADC data input, bit 1 | PDIZ | in | x |
| 17 | 11 | ADC_DATA0 | ADC data input, bit 0 (LSB) | PDIZ | in | x |
| 18 | 12 | DVSS1 | Digital ground | PVSS1Z, PVSS2Z | gnd | x |
| 19 | 13 | AVSS1 | Analog ground | PVSS3Z | gnd | x |
| 20 | 14 | XIN | Oscillator input | PDX02 | osc | |
| 21 | 15 | XOUT | Oscillator output | (PDX02) | osc | |
| 22 | 16 | AVDD1 | Analog power supply | PVDD3Z | pwr | |
| 23 | | /C_DR | C-bus data read enable | PRO04T | out | |
| 24 | 17 | /RS | Low active reset | PDIZ | in | x |
| 25 | 18 | PWM | Pulse width modulated control output | PRO04T | out | |
| 26 | | /C_DW | C-bus data write enable | PRO04T | out | |
| 27 | 19 | W_AGC | Window AGC | PRO04T | out | |
| 28 | 20 | SLI | Synchronization lock indicator | PRO04T | out | |
| 29 | | /C_PR | C-bus program read enable | PRO04T | out | |
| 30 | 21 | HSSO_WIN | HSSO window signal | PRO04T | out | |
| 31 | | /C_PW | C-bus program write enable | PRO04T | out | |
| 32 | 22 | HSSO _CLK | HSSO clock signal | PRO04T | out | |
| 33 | | /ABORT | Low active ABORT signal (pull up) | PDUZ | in | x |
| 34 | 23 | HSSO _DAT | HSSO data signal | PRO04T | out | |
| 35 | 24 | C_ADD0 | C-bus address bit 0 (LSB) | PRO04T | out | |
| 36 | 25 | C_ADD1 | C-bus address bit 1 | PRO04T | out | |
| 37 | 26 | /BOOT_RE | BOOT read enable | PRO04T | out | |
| 38 | 27 | C_ADD2 | C-bus address bit 2 | PRO04T | out | |
| 39 | 28 | C_ADD3 | C-bus address bit 3 | PRO04T | out | |
| 40 | 29 | C_ADD4 | C-bus address bit 4 | PRO04T | out | |
| 41 | 30 | C_ADD5 | C-bus address bit 5 | PRO04T | out | |
| 42 | 31 | C_ADD6 | C-bus address bit 6 | PRO04T | out | |
| 43 | | TOUT0 | Test output bit 0 | PRO02T | out | |
| 44 | 32 | C_ADD7 | C-bus address bit 7 | PRO04T | out | |

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 45 | 33 | C_ADD8 | C-bus address bit 8 | PRO04T | out | |
| 46 | 34 | C_ADD9 | C-bus address bit 9 | PRO04T | out | |
| 47 | 35 | C_ADD10 | C-bus address bit 10 | PRO04T | out | |
| 48 | 36 | C_ADD11 | C-bus address bit 11 | PRO04T | out | |
| 49 | 37 | C_ADD12 | C-bus address bit 12 | PRO04T | out | |
| 50 | 38 | DVDD1 | Digital power supply | PVDD1Z, PVDD2Z | pwr | x |
| 51 | 39 | C_ADD13 | C-bus address bit 13 | PRO04T | out | |
| 52 | | C_ADD14 | C-bus address bit 14 | PRO04T | out | |
| 53 | | C_ADD15 | C-bus address bit 15 | PRO04T | out | |
| 54 | 40 | C_DATA0/DBG | C-bus data bit 0 (pull down) | PRD04TZ | inout | x |
| 55 | 41 | C_DATA1/BOOT | C-bus data bit 1 (pull down) | PRD04TZ | inout | x |
| 56 | | C_DATA8 | C-bus data bit 8 (pull down) | PRD04TZ | inout | x |
| 57 | | C_DATA9 | C-bus data bit 9 (pull down) | PRD04TZ | inout | x |
| 58 | 42 | DVSS2 | Digital ground | PVSS1Z, PVSS2Z | gnd | x |
| 59 | 43 | C_DATA2/URST | C-bus data bit 2 (pull down) | PRD04TZ | inout | x |
| 60 | 44 | C_DATA3/XUSE | C-bus data bit 3 (pull down) | PRD04TZ | inout | x |
| 61 | | C_DATA10 | C-bus data bit 10 (pull down) | PRD04TZ | inout | x |
| 62 | | C_DATA11 | C-bus data bit 11 (pull down) | PRD04TZ | inout | x |
| 63 | 45 | C_DATA4/PSPC | C-bus data bit 4 (pull down) | PRD04TZ | inout | x |
| 64 | 46 | C_DATA5/RDI_VBIT | C-bus data bit 5 (pull down) | PRD04TZ | inout | x |
| 65 | | C_DATA12 | C-bus data bit 12 (pull down) | PRD04TZ | inout | x |
| 66 | | C_DATA13 | C-bus data bit 13 (pull down) | PRD04TZ | inout | x |
| 67 | 47 | C_DATA6/XO12 | C-bus data bit 6 (pull down) | PRD04TZ | inout | x |
| 68 | 48 | C_DATA7/ADE | C-bus data bit 7 (pull down) | PRD04TZ | inout | x |
| 69 | | C_DATA14 | C-bus data bit 14 (pull down) | PRD04TZ | inout | x |
| 70 | | C_DATA15 | C-bus data bit 15 (pull down) | PRD04TZ | inout | x |
| 71 | 49 | TEST_MODE/BYPP | Test mode selection (pull down) | PDDZ | in | x |
| 72 | 50 | MCM_TRIGGER | MCM trigger signal | PRO04T | out | |
| 73 | 51 | MC_MODE | Microcontroller mode signal | PDIZ | in | x |
| 74 | 52 | MC_CLK | Microcontroller clock signal | PDIZ | in | x |
| 75 | 53 | MC_DAT | Microcontroller data signal | PRB04TZ | inout | x |
| 76 | | DVDDE | Digital power supply | PVDD1Z, PVDD2Z | pwr | x |
| 77 | 54 | SPDIF | SPDIF output | PRO04T | out | |
| 78 | 55 | RS232 | RS232 output | PRO04T | out | |
| 79 | 56 | I2S_CLK | I2S clock output | PRO04T | out | |
| 80 | 57 | I2S_DAT | I2S data output | PRO04T | out | |
| 81 | | TOUT1 | Test output bit 1 | PRO02T | out | |
| 82 | 58 | I2S_WIN | I2S win output | PRO04T | out | |
| 83 | | TOUT2 | Test output bit 2 | PRO02T | out | |
| 84 | 59 | TOUT3 | Test output bit 3 | PRO02T | out | |
| 85 | 60 | RDI_RX | RDI receive data | PDIZ | in | x |
| 86 | 61 | RDI_TX | RDI transmit data | PRO04T | out | |
| 87 | 62 | DVSS3 | Digital ground | PVSS1Z, PVSS2Z | gnd | x |
| 88 | | TOUT4 | Test output bit 4 | PRO02T | out | |

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 89 | | TOUT5 | Test output bit 5 | PRO02T | out | |
| 90 | 63 | SFCO_SID | SFCO sub-channel ID | PRO04T | out | |
| 91 | 64 | SFCO_ERR | SFCO errorflag | PRO04T | out | |
| 92 | 65 | SFCO_DAT | SFCO data | PRO04T | out | |
| 93 | | TOUT6 | Test output bit 6 | PRO02T | out | |
| 94 | 66 | SFCO_CLK | SFCO clock | PRO04T | out | |
| 95 | 67 | SFCO_WIN | SFCO window | PRO04T | out | |
| 96 | | TOUT7 | Test output bit 7 | PRO02T | out | |
| 97 | 68 | DVDD2 | Digital power supply | PVDD1Z, PVDD2Z | pwr | x |
| 98 | 69 | TOUT8 | Test output bit 8 | PRO02T | out | |
| 99 | | TOUT9 | Test output bit 9 | PRO02T | out | |
| 100 | 70 | SRAM_D7 | SRAM data bit 7 | PRB04TZ | inout | x |
| 101 | 71 | SRAM_D6 | SRAM data bit 6 | PRB04TZ | inout | x |
| 102 | | TOUT10 | Test output bit 10 | PRO02T | out | |
| 103 | 72 | SRAM_D5 | SRAM data bit 5 | PRB04TZ | inout | x |
| 104 | 73 | SRAM_D4 | SRAM data bit 4 | PRB04TZ | inout | x |
| 105 | | TOUT11 | Test output bit 11 | PRO02T | out | |
| 106 | 74 | SRAM_D3 | SRAM data bit 3 | PRB04TZ | inout | x |
| 107 | 75 | SRAM_D2 | SRAM data bit 2 | PRB04TZ | inout | x |
| 108 | | TOUT12 | Test output bit 12 | PRO02T | out | |
| 109 | 76 | SRAM_D1 | SRAM data bit 1 | PRB04TZ | inout | x |
| 110 | 77 | SRAM_D0 | SRAM data bit 0 | PRB04TZ | inout | x |
| 111 | | TIN5 | Test input 5 (pull down) | PDDZ | in | x |
| 112 | 78 | SRAM_WR | SRAM write signal | PRO04T | out | |
| 113 | 79 | SRAM_OE | SRAM output enable | PRO04T | out | |
| 114 | 80 | SRAM_A18 | SRAM address bit 18 | PRO04T | out | |
| 115 | | TIN6 | Test input 6 (pull down) | PDDZ | in | x |
| 116 | 81 | SRAM_A17 | SRAM address bit 17 | PRO04T | out | |
| 117 | 82 | SRAM_A16 | SRAM address bit 16 | PRO04T | out | |
| 118 | | TOUT13 | Test output bit 13 | PRO02T | out | |
| 119 | 83 | SRAM_A15 | SRAM address bit 15 | PRO04T | out | |
| 120 | 84 | SRAM_A14 | SRAM address bit 14 | PRO04T | out | |
| 121 | 85 | DVSS4 | Digital ground | PVSS1Z, PVSS2Z | gnd | x |
| 122 | | TIN7 | Test input 7 (pull down) | PDDZ | in | x |
| 123 | 86 | SRAM_A13 | SRAM address bit 13 | PRO04T | out | |
| 124 | 87 | SRAM_A12 | SRAM address bit 12 | PRO04T | out | |
| 125 | | TOUT14 | Test output bit 14 | PRO02T | out | |
| 126 | 88 | SRAM_A11 | SRAM address bit 11 | PRO04T | out | |
| 127 | 89 | SRAM_A10 | SRAM address bit 10 | PRO04T | out | |
| 128 | | TOUT15 | Test output bit 15 | PRO02T | out | |
| 129 | 90 | SRAM_A9 | SRAM address bit 9 | PRO04T | out | |
| 130 | 91 | SRAM_A8 | SRAM address bit 8 | PRO04T | out | |

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 131 | | TOUT16 | Test output bit 16 | PRO02T | out | |
| 132 | 92 | SRAM_A7 | SRAM address bit 7 | PRO04T | out | |
| 133 | 93 | SRAM_A6 | SRAM address bit 6 | PRO04T | out | |
| 134 | 94 | DVDD3 | Digital power supply | PVDD1Z, PVDD2Z | pwr | |
| 135 | | TOUT17 | Test output bit 17 | PRO02T | out | |
| 136 | 95 | SRAM_A5 | SRAM address bit 5 | PRO04T | out | |
| 137 | 96 | SRAM_A4 | SRAM address bit 4 | PRO04T | out | |
| 138 | | TMUX0 | Test mux in bit 0 (LSB) (pull down) | PDDZ | in | x |
| 139 | 97 | SRAM_A3 | SRAM address bit 3 | PRO04T | out | |
| 140 | 98 | SRAM_A2 | SRAM address bit 2 | PRO04T | out | |
| 141 | | TMUX1 | Test mix in bit 1 (pull down) | PDDZ | in | x |
| 142 | 99 | SRAM_A1 | SRAM address bit 1 | PRO04T | out | |
| 143 | 100 | SRAM_A0 | SRAM address bit 0 | PRO04T | out | |
| 144 | | TMUX2 | Test mux in bit 2 (pull down) | PDDZ | in | x |

# 4 Strap Pins

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir | Comment |
|---|---|---|---|---|---|---|
| 16 | 10 | ADC_DATA1 | ADC data input, bit 1 | PDIZ | in | Strap pin OCSEL 1 |
| 17 | 11 | ADC_DATA0 | ADC data input, bit 0 | PDIZ | in | Strap pin OCSEL 0 |
| 54 | 40 | C_DATA0/DBG | C-bus data bit 0 | PRD04TZ | inout | Strap pin C_DATA0/DBG |
| 55 | 41 | C_DATA1/BOOT | C-bus data bit 1 | PRD04TZ | inout | Strap pin C_DATA1/BOOT |
| 59 | 43 | C_DATA2/URST | C-bus data bit 2 | PRD04TZ | inout | Strap pin C_DATA2/URST |
| 60 | 44 | C_DATA3/XUSE | C-bus data bit 3 | PRD04TZ | inout | Strap pin C_DATA3/XUSE |
| 63 | 45 | C_DATA4/PSPC | C-bus data bit 4 | PRD04TZ | inout | Strap pin C_DATA4/PSPC |
| 64 | 46 | C_DATA5/<br>RDI_VBIT | C-bus data bit 5 | PRD04TZ | inout | Strap pin C_DATA5/RDI_VBIT<br>0 RDI spec.: validity bit 1<br>1 IEC958 spec.: validity bit 0 |
| 67 | 47 | C_DATA6/XO12 | C-bus data bit 6 | PRD04TZ | inout | Strap pin C_DATA6/XO12<br>0 external oscillator 24.576 MHz<br>1 external oscillator 12.288 MHz |
| 68 | 48 | C_DATA7/ADE | C-bus data bit 7<br>ADC_DATA strap pin function enable | PRD04TZ | inout | Strap pin C_DATA7/ADE<br>0 ADC_DATA strap pin function disabled<br>1 ADC_DATA strap pin function enabled |
| 71 | 49 | TEST_MODE/BYPP | Test mode selection | PDDZ | in | Strap pin TEST_MODE/BYPP<br>0 PLL activated<br>1 PLL bypassed |
| 73 | 51 | MC_MODE | Microcontroller mode signal | PDIZ | in | Strap pin I2C/L3<br>0 I2C<br>1 L3 |

# 5 Pin Configuration

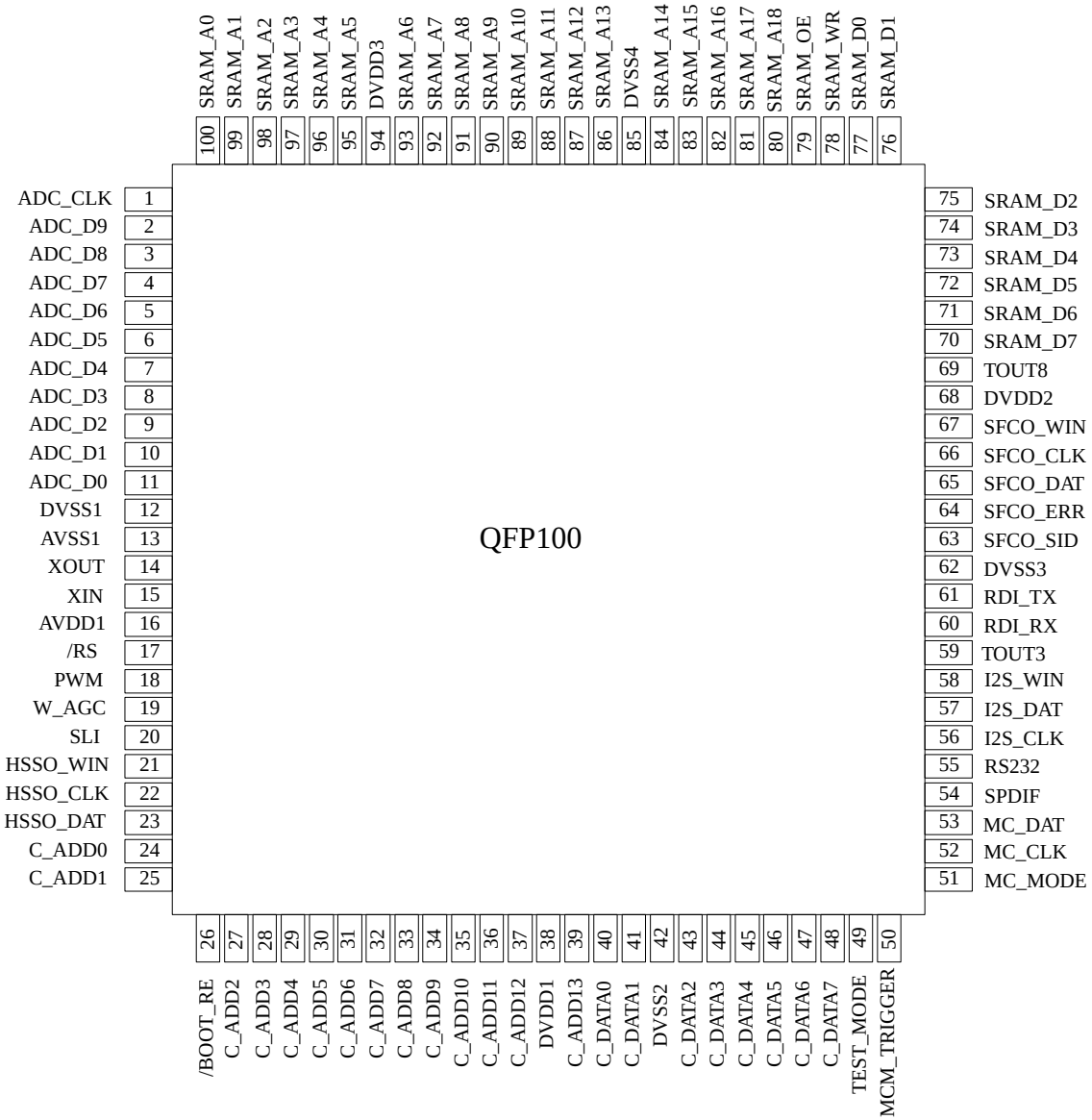



Figure 3. Production version QFP100

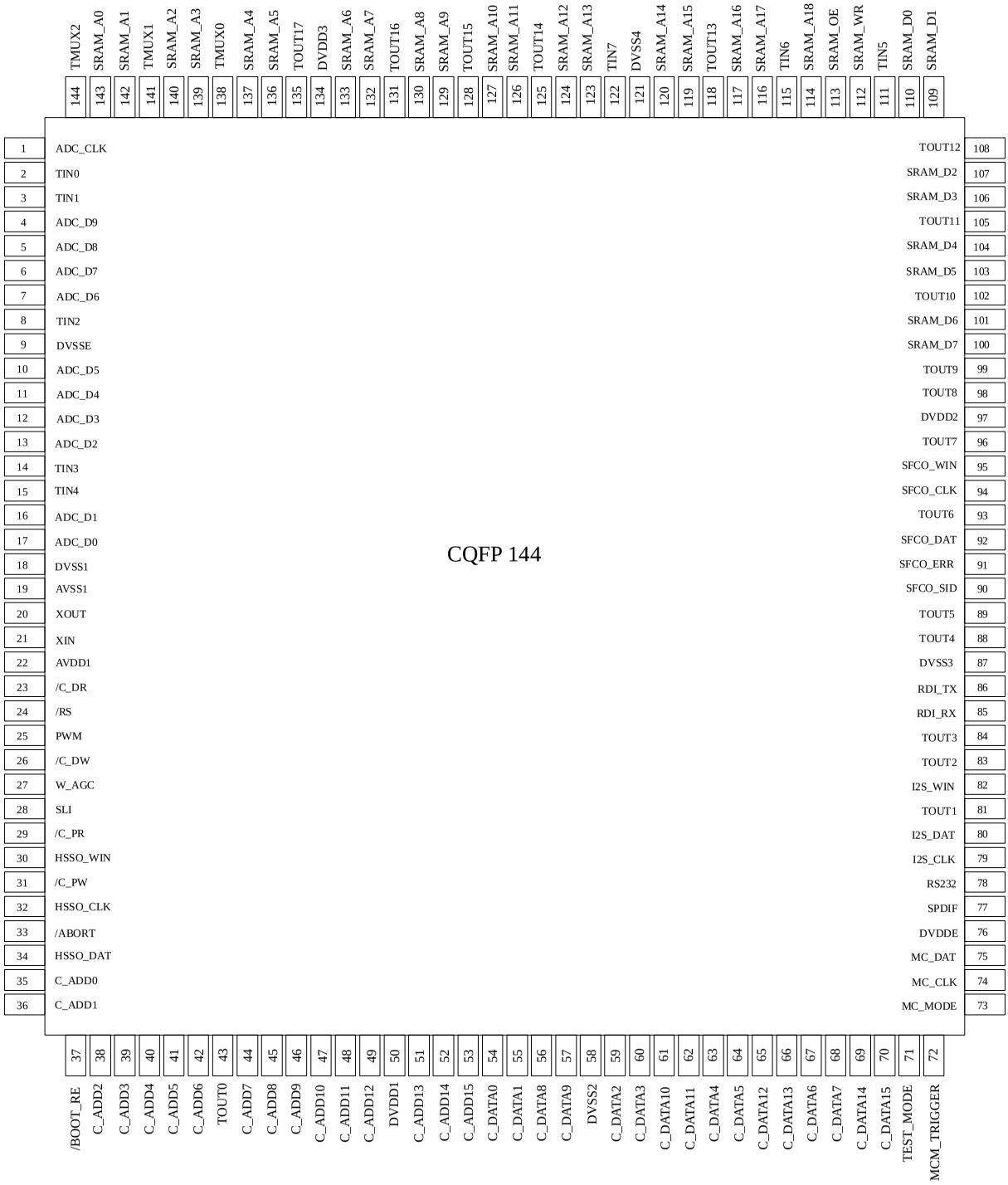



Figure 4. Software development version QFP144

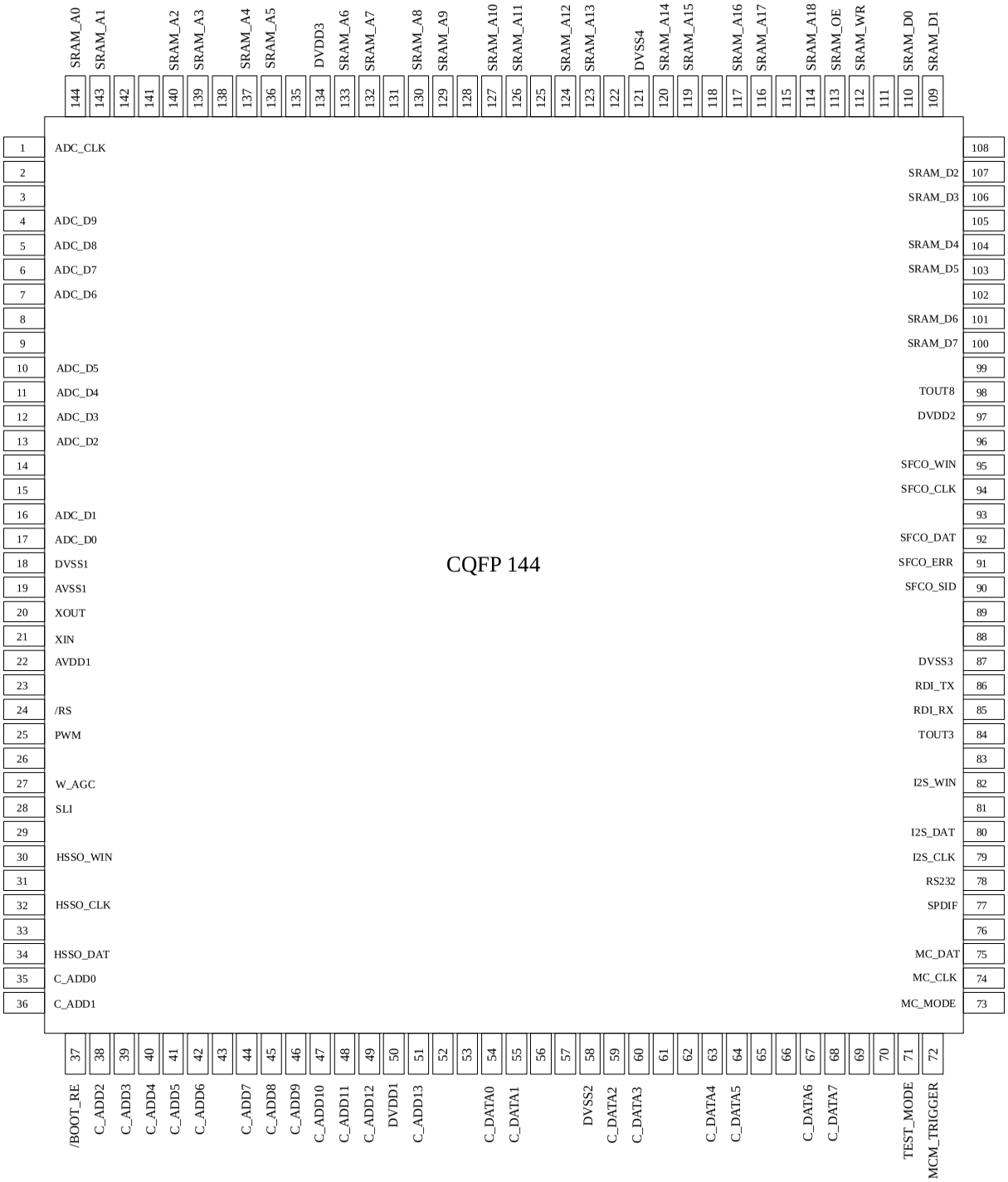



Figure 5. Version QFP144 used as production version

# 6 Interface Description

## 6.1 Overview

The interface description explains the purpose, the utilization and the meaning of every interface and every signal. It is divided into twelve sections, which are related to the different interfaces. An overview of all interfaces is shown in the functional block diagram below. Several standard output interfaces like $I^2S$ or SPDIF are used to offer a flexible usage of the U2739M-B.

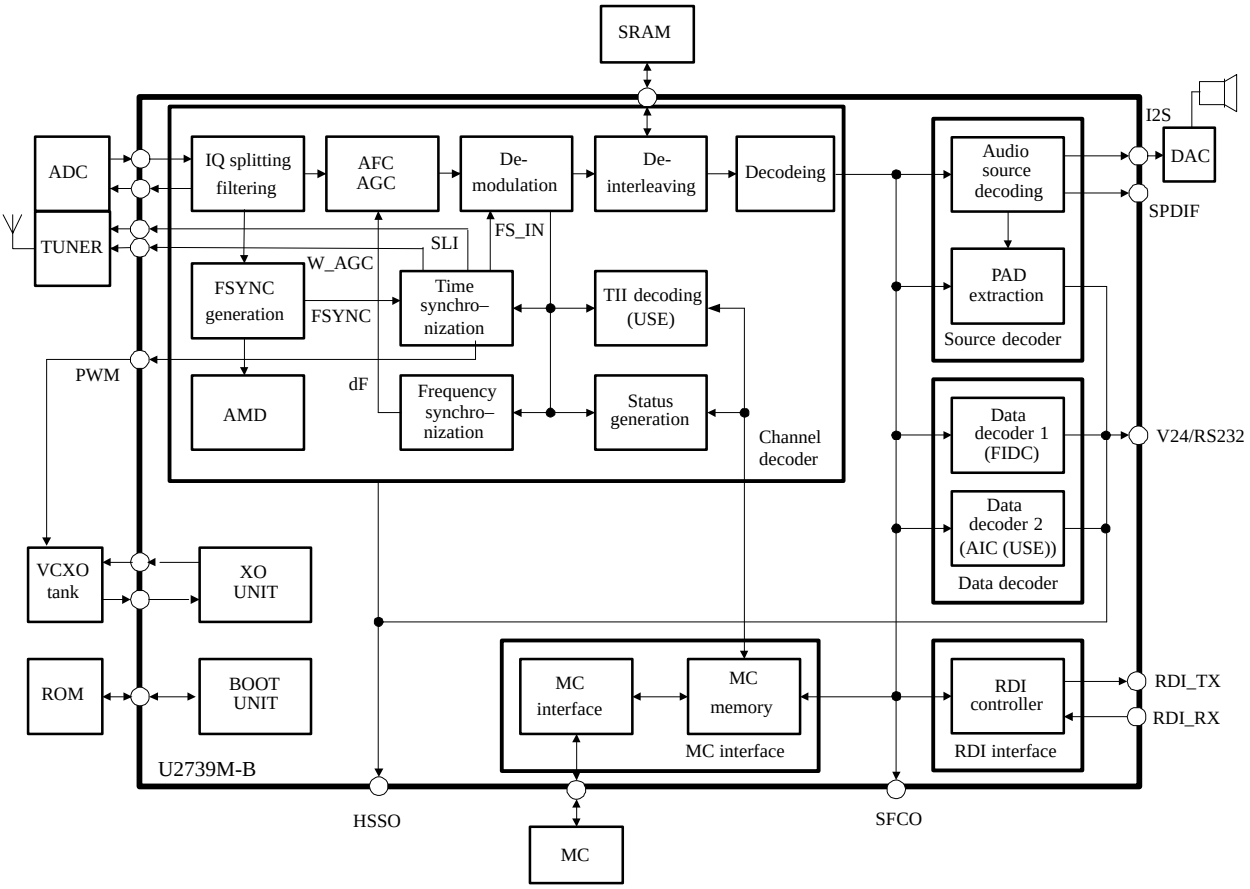



Figure 6. Functional block diagram

## 6.2 ADC Interface

### 6.2.1 ADC Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 1 | 1 | ADC_CLK | ADC sampling clock output 8.192 MHz | PDO04T | out | |
| 4 | 2 | ADC_DATA9 | ADC data input, bit 9 (MSB) | PDIZ | in | x |
| 5 | 3 | ADC_DATA8 | ADC data input, bit 8 | PDIZ | in | x |
| 6 | 4 | ADC_DATA7 | ADC data input, bit 7 | PDIZ | in | x |
| 7 | 5 | ADC_DATA6 | ADC data input, bit 6 | PDIZ | in | x |
| 10 | 6 | ADC_DATA5 | ADC data input, bit 5 | PDIZ | in | x |
| 11 | 7 | ADC_DATA4 | ADC data input, bit 4 | PDIZ | in | x |
| 12 | 8 | ADC_DATA3 | ADC data input, bit 3 | PDIZ | in | x |
| 13 | 9 | ADC_DATA2 | ADC data input, bit 2 | PDIZ | in | x |
| 16 | 10 | ADC_DATA1 | ADC data input, bit 1 | PDIZ | in | x |
| 17 | 11 | ADC_DATA0 | ADC data input, bit 0 (LSB) | PDIZ | in | x |

### 6.2.2 ADC Interface Description

The ADC interface as shown in figure 6 consists of the ADC data input signal ADC_DATA(9:0) and the ADC sampling clock output signal ADC_CLK. The U2739M-B can be connected to every standard AD with either binary or 2's complement output format. The sampling frequency is 8.192 MHz and a bandwidth of 2 MHz is necessary. The possible IF's, which are supported in conjunction with the IF input signal mode (parameter IFM) are given by the formula.

$f_{if}$ = 2.048 MHz + n × 4.096 MHz, with n = 0, 1, 2, 3 ....

Thus possible IFs are 2.048 MHz, 6.144 MHz, ... 38.912 MHz. The parameter IFM is defined by the MC command 'set global configuration' [Atmel Wireless & Microcontrollers U2739M documentation set – "U2739M_MC_Command_set_vxxx.pdf"]. The analog input bandwidth of the A/D converter must be chosen accordingly. The ADC_DATA input is 10 bit wide. The typical output delay (td3 in figure 7) of the AD converter related to the falling edge of the sampling clock CLK8192 should be 20 ns. The generated 8.192 MHz output clock take over the ADC_DATA with his rising edge of ADC_CLK. The format 'binary offset' or '2's complement' of the A/D converter can be selected by the parameter ADCF. This parameter is also defined by the 'set global configuration' MC command [Atmel Wireless & Microcontrollers U2739M documentation set – "U2739M_MC_Command_set_vxxx.pdf"].

Furthermore, the sampling clock generation is performed by the U2739M-B. The input data appearing at the ADC_DATA port are assumed to be generated by an A/D converter. The effective resolution of this converter should be greater than 9 bit in order to use the full dynamic range implemented in the U2739M-B. The sampling clock required for the external A/D converter is derived inside U2739M-B. It has to be 8.192 MHz.

### 6.2.3 ADC Interface Timing Diagram

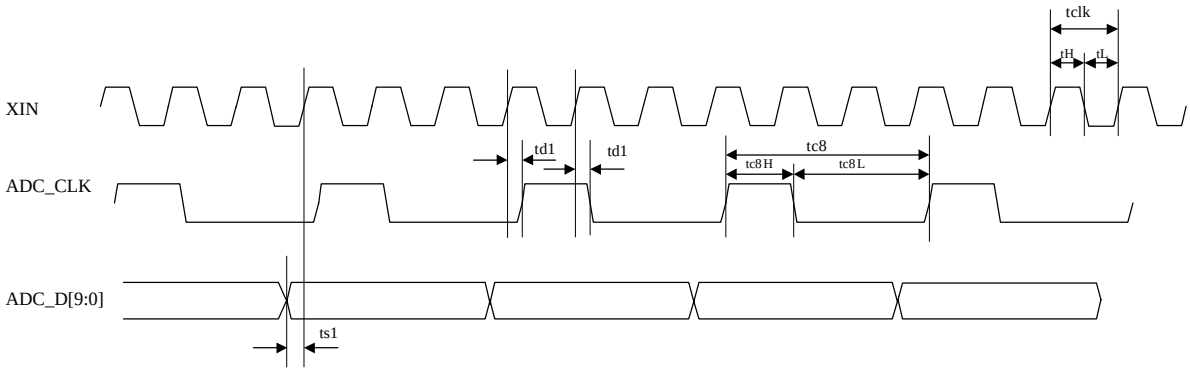



Figure 7. ADC interface timing diagram

### 6.2.4 ADC Interface Timing Parameters

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| XIN clock period | tclk | | 40.7 | | ns |
| XIN clock high | tH | 15.0 | 20.35 | 25.0 | ns |
| XIN clock low | tL | 15.0 | 20.35 | 25.0 | ns |
| ADC_CLK clock period | tc8 | | 3 × 40.7 | | ns |
| ADC_CLK clock high | tc8H | | 1 × 40.7 | | ns |
| ADC_CLK clock low | tc8L | | 2 × 40.7 | | ns |
| Setup time ADC_D(9:0) | ts1 | 5.0 | | | ns |
| Output delay of ADC_CLK | td1 | 12.0 | 20.0 | 28.0 | ns |

## 6.3 Tuner Interface

### 6.3.1 Tuner Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 27 | 19 | W_AGC | Window AGC<br>0 during COFDM symbols<br>1 during the NULL symbol | PRO04T | out | |
| 28 | 20 | SLI | Synchronization lock indicator<br>0 receiver synchronization not locked<br>1 receiver synchronization locked | PRO04T | out | |

### 6.3.2 Tuner Interface Description

In order to implement a flexible AGC concept of a DAB receiver the signals W_AGC and SLI can be used to control the tuner IC U2731B. The influence of W_AGC and SLI to the RF AGC voltage generation block is described in the U2731B preliminary datasheet.

The WAGC signal must be controlled by the MC by using the set WAGC configuration MC command. The WAGC signal does not follow the moving FFT window. The rising and falling edge can be adjusted by the MC. The MC can use the differential dT, which correspond to the FFT window shift, from the read synchronization status command to adjust the WAGC rising and falling edge.

## 6.4 MC Interface

### 6.4.1 MC Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 72 | 50 | MCM_TRIGGER | MCM trigger signal | PRO04T | out | |
| 73 | 51 | MC_MODE | Microcontroller mode signal<br>0 I2C bus protocol<br>1 L3 bus protocol | PDIZ | in | x |
| 74 | 52 | MC_CLK | Microcontroller clock signal | PDIZ | in | x |
| 75 | 53 | MC_DAT | Microcontroller data signal | PRB04TZ | inout | x |

### 6.4.2 MC Interface Description

The MC interface is used for data transmission between the U2739M-B (slave) and an external microcontroller (master). It can be configured for L3- or I2C protocol depending on the status of the MC_MODE line during reset (/RS = LOW):

MC_MODE = HIGH □ L3 bus selected

MC_MODE = LOW □ I2C bus selected

The MCM_TRIGGER line indicates the status of the internal interface controller.

The external MCU is able to communicate with the U2739M-B during LOW phases of MCM_TRIGGER only !

Further the MCM trigger signal indicates the synchronization status. If the MCM trigger has period of 8 ms, then the U2739M-B is not locked. In the synchronized (‘locked’) state the MCM trigger period correspond to the CIF frame, which is provided every 24 ms. The complete FIC is processed at the beginning of the transmission frame.

### 6.4.3 L3 Bus Interface Timing Diagram

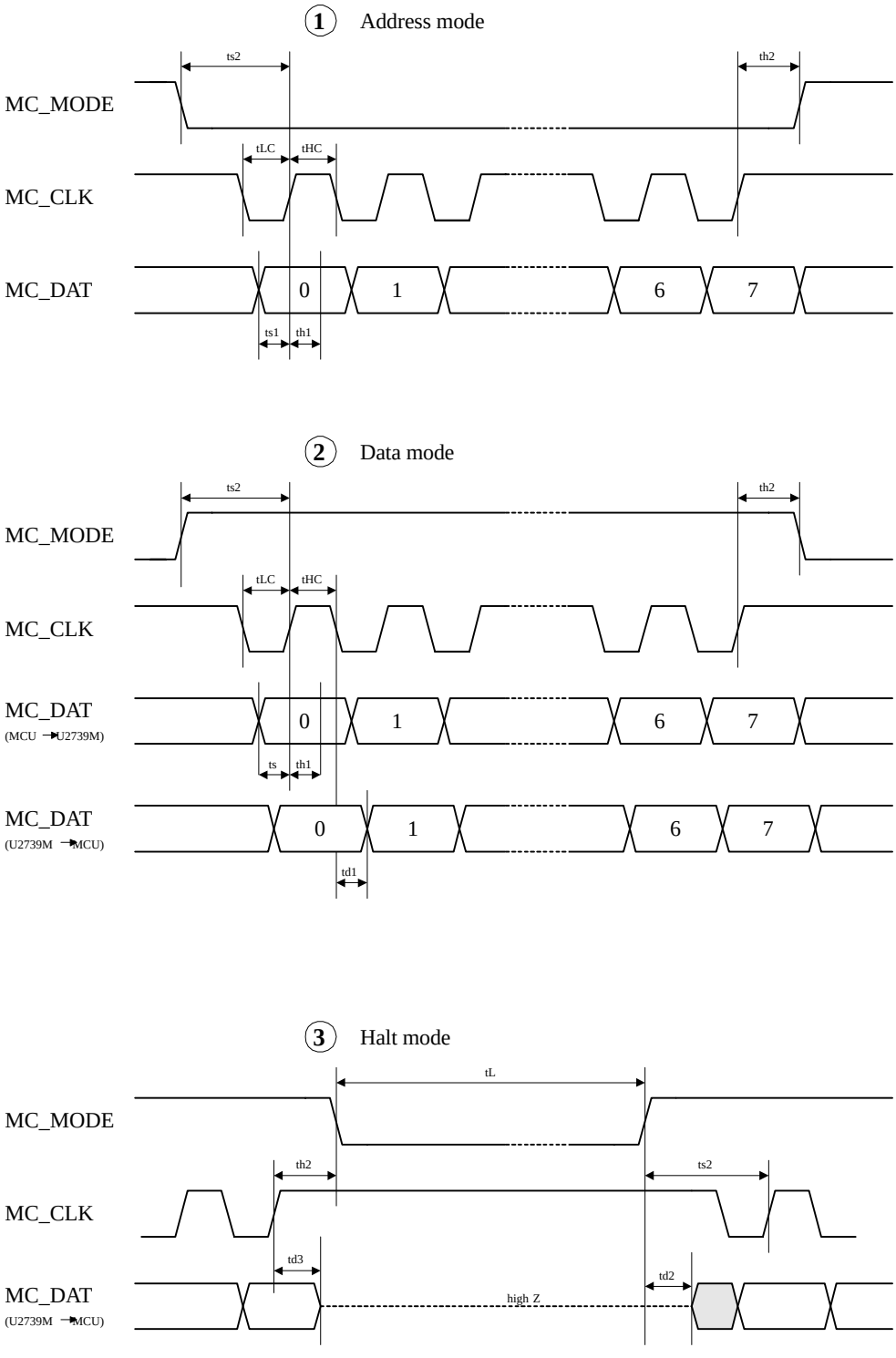



Figure 8. MC L3 bus interface timing diagram

### 6.4.4 L3 Bus Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| MC_CLK low phase | tLC | 61 | | | ns |
| MC_CLK high phase | tHC | 61 | | | ns |
| MC_DAT input setup time | ts1 | 61 | | | ns |
| MC_DAT input hold time | th1 | 61 | | | ns |
| MC_MODE hold time | th2 | 61 | | | ns |
| MC_MODE setup time | ts2 | 61 | | | ns |
| MC_CLK(h/l) / MC_DAT delay | td1 | 20 | | 100 | ns |
| MC_MODE(l/h) / MC_DAT (output driven) | td2 | 110 | | 130 | ns |
| MC_CLK(l/h) / MC_DAT(high Z) | td3 | 120 | | 160 | ns |

### 6.4.5 I2C Bus Interface Timing Diagram

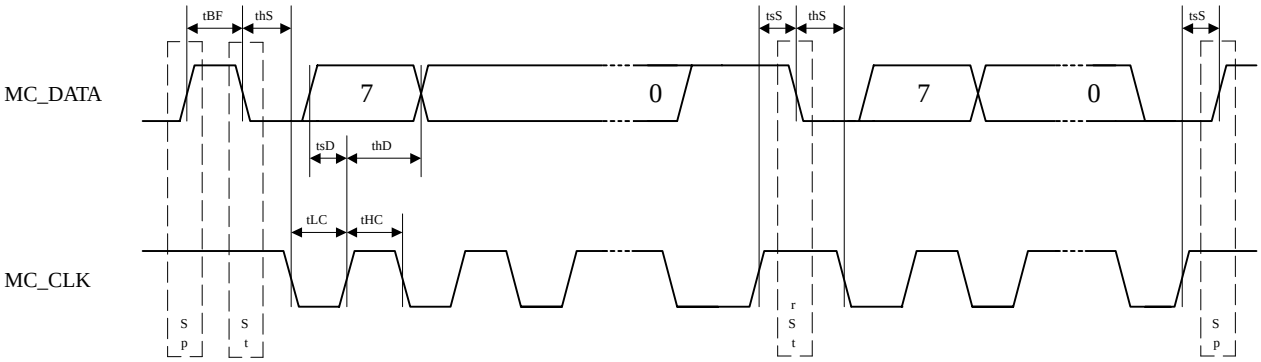



Figure 9. MC I2C bus timing diagram

### 6.4.6 I2C Bus Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Bus free time between STOP and START condition | tBF | 400 | | | ns |
| Hold time (repeated) START condition | thS | 200 | | | ns |
| Setup time data | tsD | 120 | | | ns |
| Hold time data | thD | 320 | | | ns |
| Low period clock | tLC | 300 | | | ns |
| High period clock | tHC | 200 | | | ns |
| Setup time:<br>repeated START condition, STOP condition | tsS | 240 | | | ns |

## 6.5 C-Bus / BOOT Bus Interface

### 6.5.1 C-Bus Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 23 | | /C_DR | C-bus data read enable | PRO04T | out | |
| 26 | | /C_DW | C-bus data write enable | PRO04T | out | |
| 29 | | /C_PR | C-bus program read enable | PRO04T | out | |
| 31 | | /C_PW | C-bus program write enable | PRO04T | out | |
| 35 | 24 | C_ADD0 | C-bus address bit 0 (LSB) | PRO04T | out | |
| 36 | 25 | C_ADD1 | C-bus address bit 1 | PRO04T | out | |
| 37 | 26 | /BOOT_RE | BOOT read enable | PRO04T | out | |
| 38 | 27 | C_ADD2 | C-bus address bit 2 | PRO04T | out | |
| 39 | 28 | C_ADD3 | C-bus address bit 3 | PRO04T | out | |
| 40 | 29 | C_ADD4 | C-bus address bit 4 | PRO04T | out | |
| 41 | 30 | C_ADD5 | C-bus address bit 5 | PRO04T | out | |
| 42 | 31 | C_ADD6 | C-bus address bit 6 | PRO04T | out | |
| 44 | 32 | C_ADD7 | C-bus address bit 7 | PRO04T | out | |
| 45 | 33 | C_ADD8 | C-bus address bit 8 | PRO04T | out | |
| 46 | 34 | C_ADD9 | C-bus address bit 9 | PRO04T | out | |
| 47 | 35 | C_ADD10 | C-bus address bit 10 | PRO04T | out | |
| 48 | 36 | C_ADD11 | C-bus address bit 11 | PRO04T | out | |
| 49 | 37 | C_ADD12 | C-bus address bit 12 | PRO04T | out | |
| 51 | 39 | C_ADD13 | C-bus address bit 13 | PRO04T | out | |
| 52 | | C_ADD14 | C-bus address bit 14 | PRO04T | out | |
| 53 | | C_ADD15 | C-bus address bit 15 | PRO04T | out | |
| 54 | 40 | C_DATA0/DBG | C-bus data bit 0 (pull down) | PRD04TZ | inout | x |
| 55 | 41 | C_DATA1/BOOT | C-bus data bit 1 (pull down) | PRD04TZ | inout | x |
| 56 | | C_DATA8 | C-bus data bit 8 (pull down) | PRD04TZ | inout | x |
| 57 | | C_DATA9 | C-bus data bit 9 (pull down) | PRD04TZ | inout | x |
| 59 | 43 | C_DATA2/URST | C-bus data bit 2 (pull down) | PRD04TZ | inout | x |
| 60 | 44 | C_DATA3/XUSE | C-bus data bit 3 (pull down) | PRD04TZ | inout | x |
| 61 | | C_DATA10 | C-bus data bit 10 (pull down) | PRD04TZ | inout | x |
| 62 | | C_DATA11 | C-bus data bit 11 (pull down) | PRD04TZ | inout | x |
| 63 | 45 | C_DATA4/PSPC | C-bus data bit 4 (pull down) | PRD04TZ | inout | x |
| 64 | 46 | C_DATA5/RDI_VBIT | C-bus data bit 5 (pull down) | PRD04TZ | inout | x |
| 65 | | C_DATA12 | C-bus data bit 12 (pull down) | PRD04TZ | inout | x |
| 66 | | C_DATA13 | C-bus data bit 13 (pull down) | PRD04TZ | inout | x |
| 67 | 47 | C_DATA6/XO12 | C-bus data bit 6 (pull down) | PRD04TZ | inout | x |
| 68 | 48 | C_DATA7/BYPP | C-bus data bit 7 (pull down) | PRD04TZ | inout | x |
| 69 | | C_DATA14 | C-bus data bit 14 (pull down) | PRD04TZ | inout | x |
| 70 | | C_DATA15 | C-–bus data bit 15 (pull down) | PRD04TZ | inout | x |

### 6.5.2 C-Bus / BOOT Bus Interface Description

The C-Bus is a multiplexed program as well as data bus system to communicate with external components. The complete bus system is available only in the QFP144 package version and needed for debugging the internal OAK DSP core.

The BOOT bus covers a subset of the C-Bus signals. The user is able to download his own so-called 'User Software Extensions' using this bus system to replace or extend the Atmel Wireless & Microcontrollers firmware. The BOOT bus is a standard ROM interface (address/ data buses, read enable line) and the read access is always with 16 wait states (referring the OAK internal 49.152 MHz clock) to support slow devices.

The BOOT bus is available in both package versions. The timing diagram refers to the BOOT bus signals only.

### 6.5.3 BOOT Bus Timing Diagram

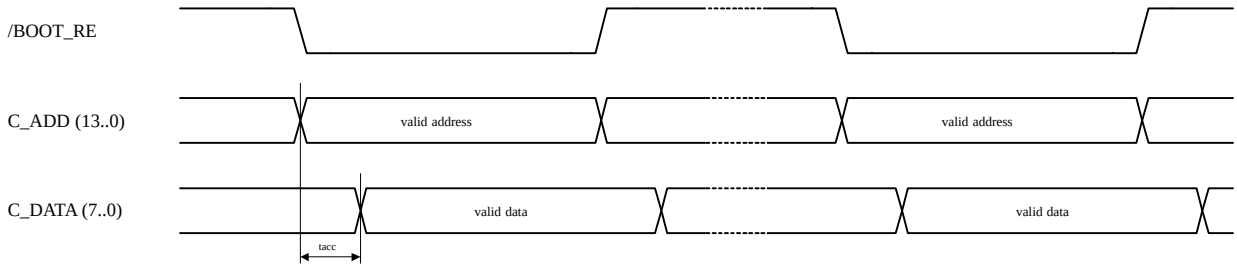



Figure 10. C-bus interface timing diagram

### 6.5.4 BOOT Bus Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| BOOT ROM access time | tacc | | | 120 | ns |

## 6.6 SRAM Interface

### 6.6.1 SRAM Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 100 | 70 | SRAM_D7 | SRAM data bit 7 | PRB04TZ | inout | x |
| 101 | 71 | SRAM_D6 | SRAM data bit 6 | PRB04TZ | inout | x |
| 103 | 72 | SRAM_D5 | SRAM data bit 5 | PRB04TZ | inout | x |
| 104 | 73 | SRAM_D4 | SRAM data bit 4 | PRB04TZ | inout | x |
| 106 | 74 | SRAM_D3 | SRAM data bit 3 | PRB04TZ | inout | x |
| 107 | 75 | SRAM_D2 | SRAM data bit 2 | PRB04TZ | inout | x |
| 109 | 76 | SRAM_D1 | SRAM data bit 1 | PRB04TZ | inout | x |
| 110 | 77 | SRAM_D0 | SRAM data bit 0 | PRB04TZ | inout | x |
| 112 | 78 | SRAM_WR | SRAM write signal | PRO04T | out | |
| 113 | 79 | SRAM_OE | SRAM output enable | PRO04T | out | |
| 114 | 80 | SRAM_A18 | SRAM address bit 18 | PRO04T | out | |
| 116 | 81 | SRAM_A17 | SRAM address bit 17 | PRO04T | out | |
| 117 | 82 | SRAM_A16 | SRAM address bit 16 | PRO04T | out | |
| 119 | 83 | SRAM_A15 | SRAM address bit 15 | PRO04T | out | |
| 120 | 84 | SRAM_A14 | SRAM address bit 14 | PRO04T | out | |
| 123 | 86 | SRAM_A13 | SRAM address bit 13 | PRO04T | out | |
| 124 | 87 | SRAM_A12 | SRAM address bit 12 | PRO04T | out | |
| 126 | 88 | SRAM_A11 | SRAM address bit 11 | PRO04T | out | |
| 127 | 89 | SRAM_A10 | SRAM address bit 10 | PRO04T | out | |
| 129 | 90 | SRAM_A9 | SRAM address bit 9 | PRO04T | out | |
| 130 | 91 | SRAM_A8 | SRAM address bit 8 | PRO04T | out | |
| 132 | 92 | SRAM_A7 | SRAM address bit 7 | PRO04T | out | |
| 133 | 93 | SRAM_A6 | SRAM address bit 6 | PRO04T | out | |
| 136 | 95 | SRAM_A5 | SRAM address bit 5 | PRO04T | out | |
| 137 | 96 | SRAM_A4 | SRAM address bit 4 | PRO04T | out | |
| 139 | 97 | SRAM_A3 | SRAM address bit 3 | PRO04T | out | |
| 140 | 98 | SRAM_A2 | SRAM address bit 2 | PRO04T | out | |
| 142 | 99 | SRAM_A1 | SRAM address bit 1 | PRO04T | out | |
| 143 | 100 | SRAM_A0 | SRAM address bit 0 | PRO04T | out | |

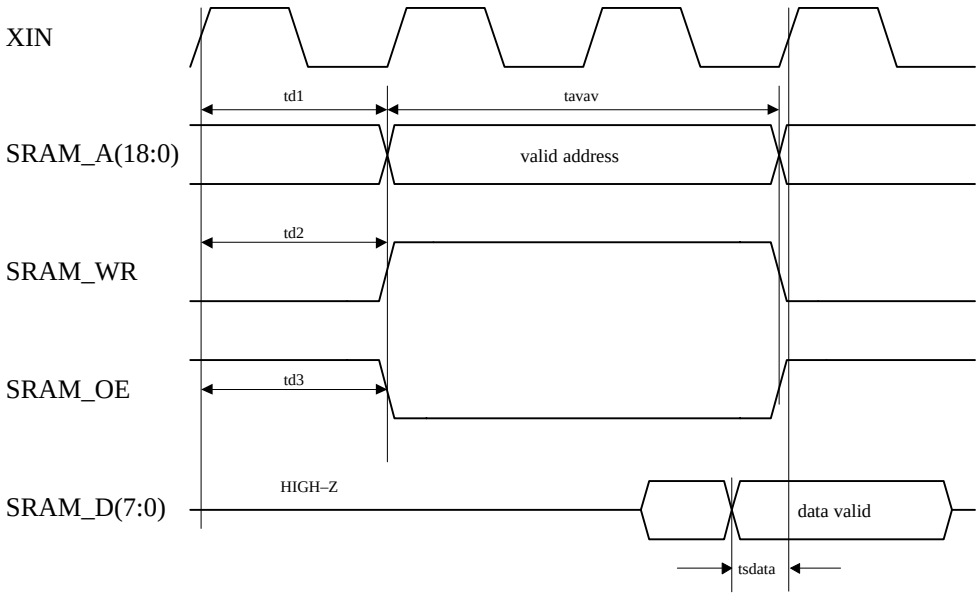
### 6.6.2 SRAM Interface Descriptions

For time de-interleaving and further task an external static random access memory of 4 MB is necessary. The organization of the SRAM is 512 k × 8 bit.

Due to the high data rates a fast SRAM with a access time of 18 ns or below is necessary.

### 6.6.3 SRAM Interface Timing Diagram

**READ CYCLE**




**WRITE CYCLE**

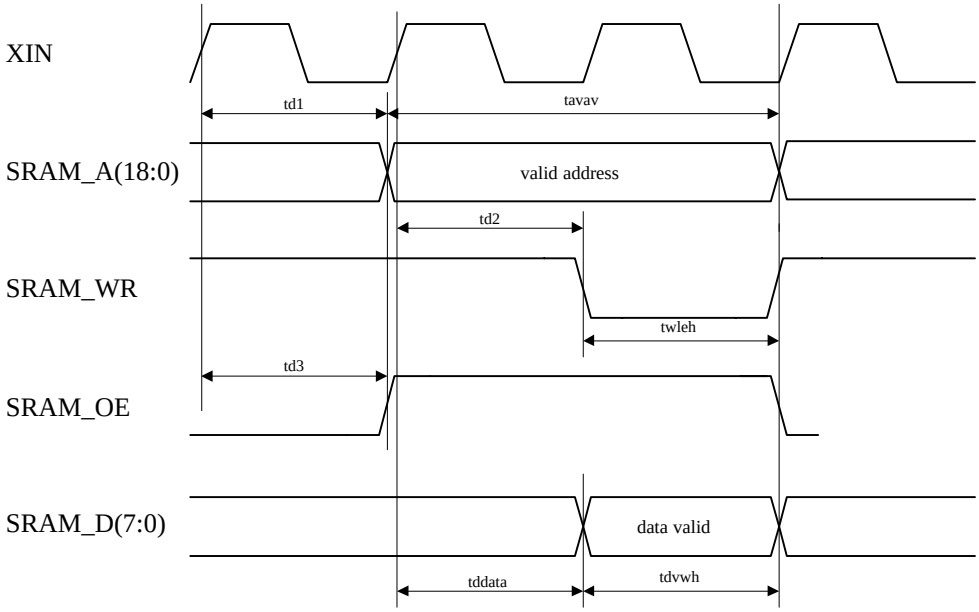



Figure 11. SRAM interface timing diagram

### 6.6.4 SRAM Interface Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Read/ write cycle time | tavav | | 40.7 | | ns |
| Output delay SRAM_A(18:0) | td1 | 15.0 | 25.0 | 35.0 | ns |
| Output delay SRAM_WR | td2 | 12.0 | 20.0 | 28.0 | ns |
| Output delay SRAM_OE | td3 | 16.0 | 24.0 | 32.0 | ns |
| Setup time SRAM_D(7:0) | tsdata | 2.0 | | | ns |
| Write pulse with | twleh | 33.0 | 40.7 | 48.0 | ns |
| Output delay SRAM_D(7:0) | tddata | 15.0 | 23.0 | 31.0 | ns |
| Data valid to end of write | tdvwh | 33.0 | 40.7 | 48.0 | ns |

## 6.7 VCXO Interface

### 6.7.1 VCXO Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 19 | 13 | AVSS1 | Analog ground | PVSS3Z | gnd | x |
| 20 | 14 | XIN | Oscillator input | PDX02 | osc | |
| 21 | 15 | XOUT | Oscillator output | (PDX02) | osc | |
| 22 | 16 | AVDD1 | Analog power supply | PVDD3Z | pwr | |
| 25 | 18 | PWM | Pulse width modulated control output | PRO04T | out | |

### 6.7.2 VCXO Interface Description

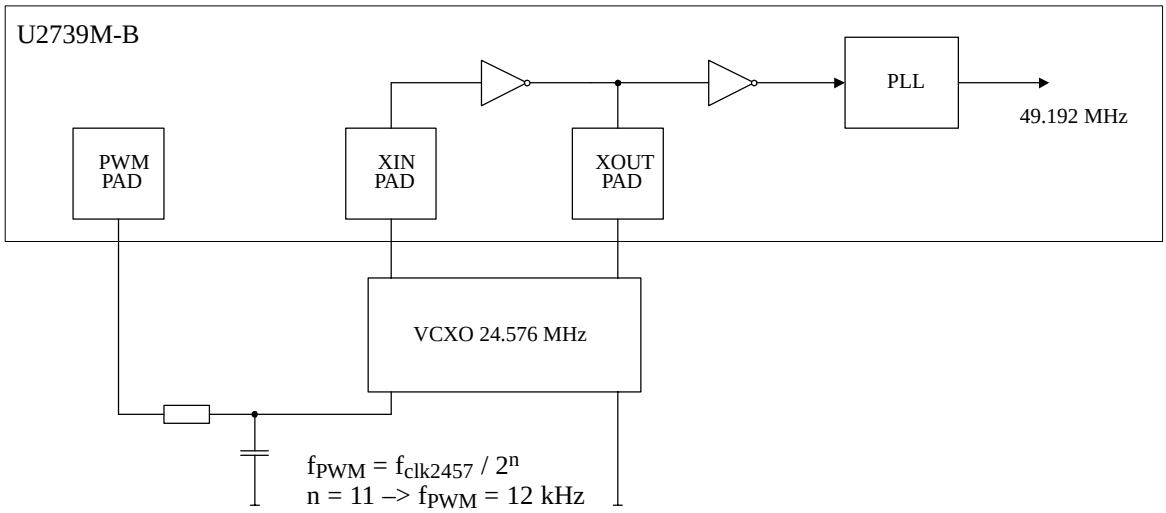



Figure 12. VCXO application circuit

The U2739M-B master clock should be derived from a voltage-controlled reference oscillator. The pulse width modulated output signal PWM of the U2739M-B can be used to control the VCXO frequency of 24.576 MHz.

## 6.8 Audio Interfaces

### 6.8.1 I2S Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 79 | 56 | I2S_CLK | I2S clock line | PRO04T | out | |
| 80 | 57 | I2S_DAT | I2S data line | PRO04T | out | |
| 82 | 58 | I2S_WIN | I2S window line | PRO04T | out | |

### 6.8.2 I2S Interface Description

The I2S interface is a standard continuous audio interface consisting of bit clock (_CLK), word select (_WIN) and data (_DAT) lines. The word select line indicates the transmitted channel: LOW for left, HIGH for right. Please be aware of the 1 cycle delay of the data word MSB corresponding to the I2S_WIN edge !

As in the DAB system the I2S_WIN clock is fixed as 48 kHz (MPEG1) or 24 kHz (MPEG2) the bit clock depends on the data word length. The standard word length is 16 bit, hence the bit clock is fixed at 1.536 MHz resp. 768 kHz.

### 6.8.3 I2S Interface Timing Diagram

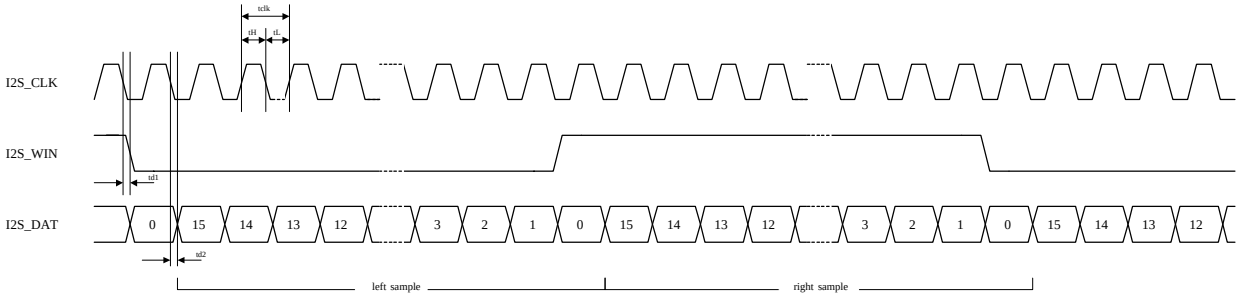



Figure 13. I2S interface timing diagram

### 6.8.4 I2S Interface Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| I2S clock period | tclk | | 16.28 | | us |
| I2S clock high | tH | | 14.28 | | us |
| I2S clock low | tL | | 14.28 | | us |
| I2S_WIN output delay | td1 | –5.0 | 0.0 | 5.0 | ns |
| I2S_DAT output delay | td2 | –5.0 | 0.0 | 5.0 | ns |

### 6.8.5 SP-DIF Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 77 | 54 | SPDIF | SPDIF output | PRO04T | out | |

### 6.8.6 SP-DIF Interface Description

The SP-DIF format is frame based, which means one frame represents one audio sampling period. Every frame comprises 2 subframes a 32 bit referring to the left and right sample. The data is transmitted in bi-phase coded format. The frame synchronization pattern are based on biphase violations and indicate whether a left or right subframe follows.

The last 4 bi-phase coded bits of each subframe represent the V (validity flag), U (user channel data), C (channel status data) and P (parity) information as described in the SP-DIF specification.

Complete frames (left and right sample according to 64 × 2 bit due to bi-phase coding) are transmitted at the audio sampling rate (48 resp. 24 kHz).

### 6.8.7 SP-DIF Interface Timing Parameter

The SP-DIF interface was designed according the digital audio interface IEC958 specification [CEI/ISO 958 Digital Audio Interface Standard].

### 6.8.8 SP-DIF Interface Timing Diagram

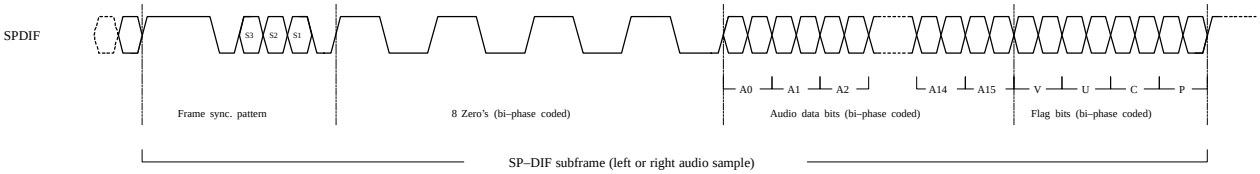



Figure 14. SP-DIF interface timing diagram

## 6.9 RDI Interface

### 6.9.1 RDI Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 64 | 46 | C_DATA5/RDI_VBIT | C–bus data bit 5 (pull down) | PRD04TZ | inout | x |
| 85 | 60 | RDI_RX | RDI receive data | PDIZ | in | x |
| 86 | 61 | RDI_TX | RDI transmit data | PRO04T | out | |

### 6.9.2 RDI Interface Description

The RDI interface is designed according to the 'Digital Audio Broadcasting System: Specification of the Receiver Data Interface (RDI)' [Digital Audio Broadcasting System: Specification of the Receiver Data Interface (RDI), Issue 1.4]. The RDI frames are embedded into the IEC 958 interface. The RDI output data is provided in the extended format of the high capacity mode. Further the RDI Control Channel (RCC) can be implemented according to the preliminary specification [Digital Audio Broadcasting System: Preliminary Specification of the RDI Control Channel], [Proposal of DAB Command Set for Receiver (DCSR)].

### 6.9.3 RDI Interface Timing Diagram

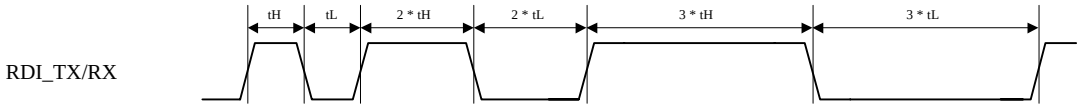



Figure 15. RDI interface timing diagram

### 6.9.4 RDI Interface Timing Parameter

The RDI interface is realized according to the digital audio interface IEC958 specification [CEI/ISO 958 Digital Audio Interface Standard].

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Data high period | TH | | 160 | | ns |
| Data low period | TL | | 160 | | ns |

## 6.10 SFCO Interface

### 6.10.1 SFCO Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 90 | 63 | SFCO_SID | SFCO sub-channel ID | PRO04T | out | |
| 91 | 64 | SFCO_ERR | SFCO error flag | PRO04T | out | |
| 92 | 65 | SFCO_DAT | SFCO data | PRO04T | out | |
| 94 | 66 | SFCO_CLK | SFCO clock | PRO04T | out | |
| 95 | 67 | SFCO_WIN | SFCO window | PRO04T | out | |

### 6.10.2 SFCO Interface Description

The simple full capacity output interface (SFCO) is a 3.072 MHz burst mode interface. It consists of a window, data, errorflag and clock line. Furthermore, a serial sub-channel identifier information is provided. The interface carries fast information channel (FIC) and main service information (MSC) at the output of the COFDM channel decoder. The window line can be used to distinguish between FIC and MSC data. Via the MC interface the provided sub-channel can be selected. Only these selected sub-channels are processed by the channel decoder.

### 6.10.3 SFCO Interface Timing Diagram

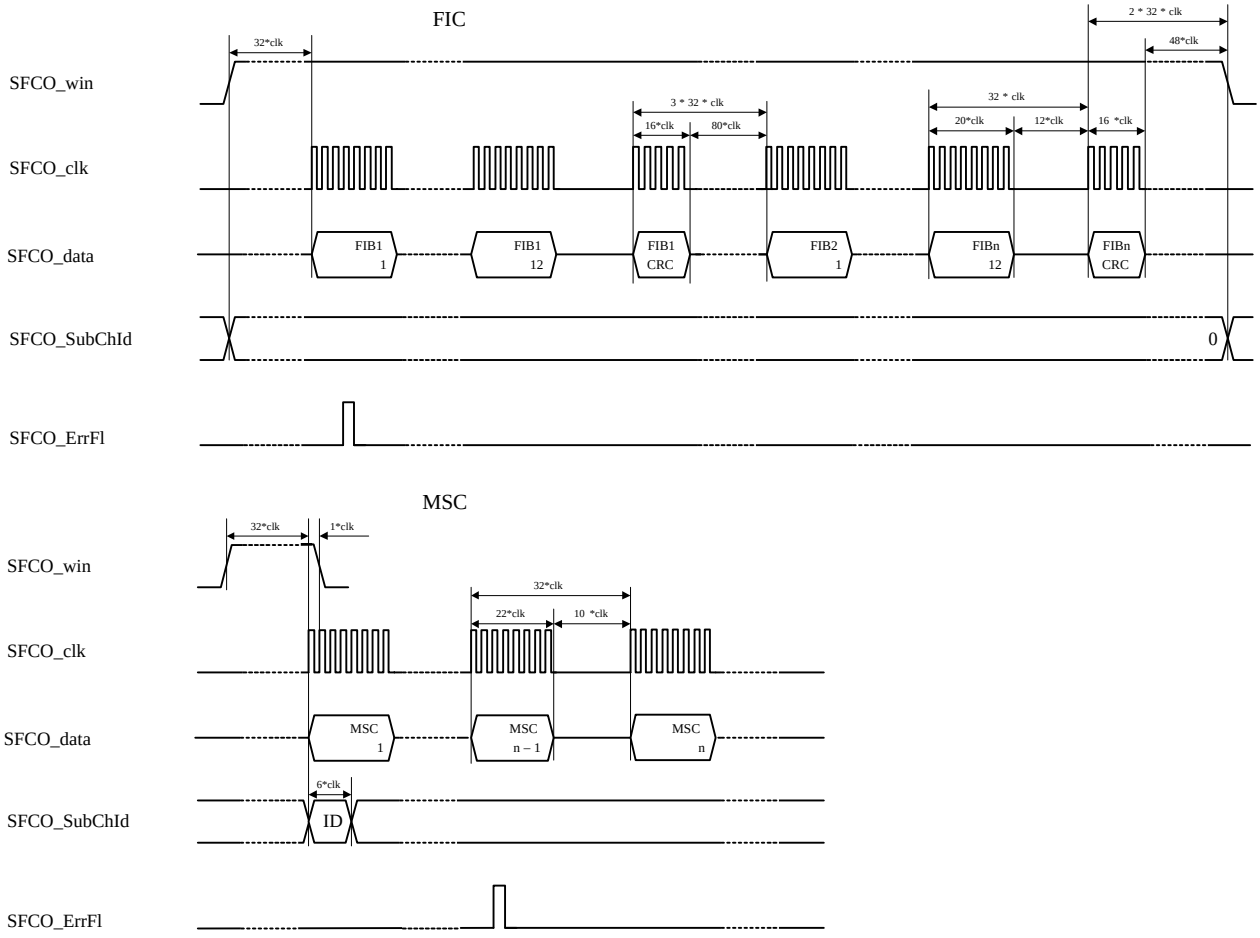



Figure 16. SFCO interface timing diagram

### 6.10.4 Detailed SFCO Interface Timing Diagram

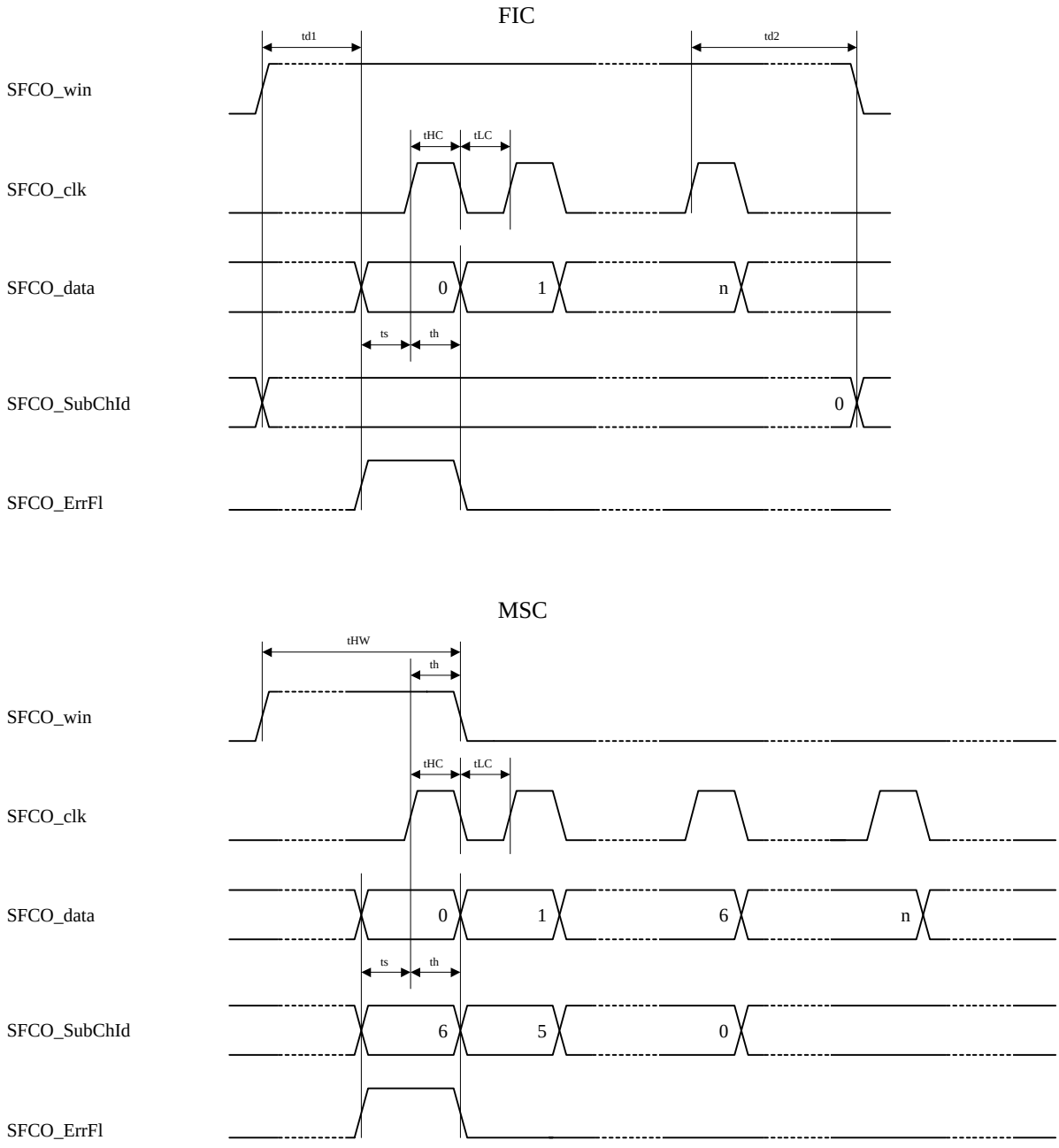



Figure 17. Detailed SFCO interface timing diagram

### 6.10.5 SFCO Interface Timing Parameter

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock high period | tHC | | 160 | | ns |
| Clock low period | tLC | | 160 | | ns |
| Data setup time | ts | | 160 | | ns |
| Data hold time | th | | 160 | | ns |
| Window MSC high period | tHW | | 10.56 | | us |
| Delay data valid | td1 | | 10.24 | | us |
| Delay window FIC low | td2 | | 10.24 | | us |

## 6.11 RS232 Interface

### 6.11.1 RS232 Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 78 | 55 | RS232 | RS232 output | PRO04T | out | |

### 6.11.2 RS232 Interface Description

The RS232 interface is an standard serial output used for transferring data directly to a PC COM port. One of 3 applications can be given out:

- Data decoder 1
- Data decoder 2
- Programme Associated Data (PAD)

Each RS232 burst consists of a header word followed by n data words (as indicated in the header):

| | RS232-ID (Burst Identifier) | | | | Length (Number of Transmitted Data Words n Without Header Word) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DD1 | 0 | 0 | 0 | 1 | Number of DD1 words | | | | | | | | | | | |
| DD2 | 0 | 0 | 1 | 0 | Number of DD2 words | | | | | | | | | | | |
| PAD | 0 | 0 | 1 | 1 | Number of PAD words | | | | | | | | | | | |

The RS232 output can be configured using the 'set HSSO/ RS232 configuration' MC command [Atmel Wireless & Microcontrollers U2739M documentation set – "U2739M_MC_Command_set_vxxx.pdf"]. Using this command the user can select the application to be given out and the baud rate.

Please notice the byte order: first the high byte is transmitted followed by the low byte (LSB first both).

### 6.11.3 RS232 Interface Timing Diagram




Figure 18. RS232 interface timing diagram

### 6.11.4 RS232 Interface Timing Parameter

The RS232 timing is related to the defined baud rate of the interface.

## 6.12 HSSO Interface

### 6.12.1 HSSO Interface Signal Description

| QFP144 | QFP100 | Pin Name | Signal Description | Pad Type | Dir. | 5 V Tol. |
|---|---|---|---|---|---|---|
| 30 | 21 | HSSO_WIN | HSSO window signal | PRO04T | out | |
| 32 | 22 | HSSO _CLK | HSSO clock signal | PRO04T | out | |
| 34 | 23 | HSSO _DAT | HSSO data signal | PRO04T | out | |

### 6.12.2 HSSO Interface Description

The High Speed Serial Output (HSSO) is a standard 3-line output interface implemented to give out data bursts in a multiplexed way. Up to 4 applications can be given out simultaneously:

- Channel Impulse Response (CIR)
- Data decoder 1
- Data decoder 2
- Programme Associated Data (PAD)

The HSSO can be configured using the 'set HSSO / RS232 configuration' MC command (see section 8). Each HSSO burst consists of a header word followed by n data words (as indicated in the header).

| | HSSO-ID (Burst Identifier) | | | | Length (Number of Transmitted Data Words n Without Header Word) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| CIR | 0 | 0 | 0 | 0 | Number of CIR words | | | | | | | | | | | |
| DD1 | 0 | 0 | 0 | 1 | Number of DD1 words | | | | | | | | | | | |
| DD2 | 0 | 0 | 1 | 0 | Number of DD2 words | | | | | | | | | | | |
| PAD | 0 | 0 | 1 | 1 | Number of PAD words | | | | | | | | | | | |

### 6.12.3 HSSO Interface Timing Diagram

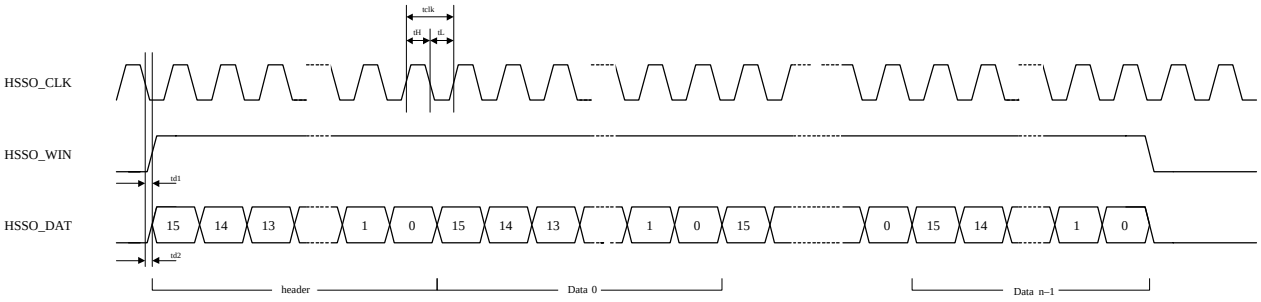



Figure 19. HSSO interface timing diagram

### 6.12.4 HSSO Interface Timing Parameters

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| HSSO clock period | tclk | | 4.07 | | us |
| HSSO clock high | tH | | 2.035 | | us |
| HSSO clock low | tL | | 2.035 | | us |
| HSSO_WIN output delay | td1 | –5.0 | 0.0 | 5.0 | ns |
| HSSO_DAT output delay | td2 | –5.0 | 0.0 | 5.0 | ns |

# 7 Electrical Characteristics

## 7.1 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | VDD | –0.5 | VDD + 0.5 | V |
| Input / output voltage | Vin/Vout | –0.5 | VDD + 0.5 | V |
| Storage temperature | Tstg | –65 | 125 | °C |

## 7.2 Operating Range

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | VDD | 3.0 | 3.3 | 3.6 | V |
| Input / output voltage | Vin/Vout | 0 | | VDD | V |
| Ambient temperature | Tamb | –40 | | +85 | °C |
| Power dissipation | Pstat | | 20 | | mW |
| Power dissipation | Pdyn | | 860 | | mW |

## 7.3 DC Characteristics

| Parameter | Test Conditions | Pad Type | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Input HIGH voltage | | VIH | | 2.0 | | | V |
| Input LOW voltage | | VIL | | | | 0.8 | V |
| Threshold | | VT | | | 1.4 | | V |
| Output HIGH voltage | IOH= –2 mA | VOH | Pxx02x | 2.4 | | VDD | V |
| | IOH= –4 mA | | Pxx04x | 2.4 | | VDD | V |
| Output LOW voltage | IOL= 2 mA | VOL | Pxx02x | | 0.2 | 0.4 | V |
| | IOL= 4 mA | | Pxx04x | | 0.2 | 0.4 | V |

# 8 MC Command Set

## 8.1 'Set System' Commands

### 8.1.1 Set DAB System Mode

Command Settings Overview:

- Set system mode
- Set FSLI control loops

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $00 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| SMODE | | NSM | 0 | 0 | 0 | 0 | 0 | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| SMODE(1..0) | New DAB system mode | 00: DAB system mode 4<br>01: DAB system mode 1<br>10: DAB system mode 2<br>11: DAB system mode 3 |
| NSM | New system mode valid | 0: SMODE not valid<br>1: SMODE indicates new system mode |

### 8.1.2 Set ASD

Command Settings Overview:

- Set ASD on/off
- Set ASD mute state
- Set ASD sub–channel ID
- Set ASD dynamic range control on/off
- Set ASD dynamic range control fixed value
- Set ASD ScF–CRC on/off
- Set ASD dual channel configuration
- Set ASD fader value

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | $10 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| ASDE | MUTE | IDV | DCCV | FADV | DRCON | DRCFIX | SCFON | $XX |
| FADD | | SBCHID | | | | | | $XX |
| DCC | | DRCFV | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| ASDE | ASD enable | 0: ASD disabled<br>1: ASD enabled |
| MUTE | ASD mute state | 0: ASD output active<br>1: ASD output muted |
| IDV | ASD SBCHID valid | 0: Last set ASD SBCHID remains valid<br>1: Following ASD SBCHID valid |
| DCCV | DCC setting valid | 0: Last set DCC remains valid<br>1: Following DCC valid |
| FADV | Fader setting valid | 0: Last set FAD remains valid<br>1: Following FAD valid |
| DRCON | DRC on/off switch | 0: DRC off<br>1: DRC on |
| DRCFIX | DRC additional fixed gain value valid | 0: DRC additional fixed gain + 6 dB (default)<br>1: DRC additional fixed gain according to DRCFV |
| SCFON | ScF–CRC on/off switch | 0: ScF–CRC off<br>1: ScF–CRC on |
| FAD | Fader value | 00: Fade In / Fade out over 0 frames each<br>01: Fade In / Fade out over 30 frames each<br>10: Fade In / Fade out over 60 frames each<br>11: Fade In / Fade out over 90 frames each |
| SBCHID(5..0) | Sub–channel identifier | n: ASD sub–channel ID |
| DCC(1..0) | Dual channel configuration | 00/10: Left channel on both ASD output channels<br>01: Right channel on both ASD output channels<br>11: Both channels on ASD output |
| DRCFV(5..0) | DRC additional fixed gain value | 000000: Fixed gain 0 dB<br>000001: Fixed gain + 0.25 dB<br>... (continuous steps of +0.25 dB)<br>111111: fixed gain + 15.75 dB |

### 8.1.3 Set DD1

DD configuration for transmission in packet mode

Command Settings Overview:

- Set DD1 on/off
- Set DD1 sub–channel ID
- Set DD1 packet address

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| DAB | | | U2739M-B | | | Write Command | |

\$6E

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

\$11

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| DAB | | | U2739M-B | | | Write Command | |

\$6C

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| DD1E | FIDC | PA1V | ID1V | 0 | | PA(9/8) | |
| PA(7..0) | | | | | | | |
| 0 | | SBCHID | | | | | |

\$XX
\$XX
\$XX

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| DD1E | DD1 enable | 0: DD1 disabled<br>1: DD1 enabled |
| FIDC | FIDC decoding switch | 0: DD1 decodes MSC<br>1: DD1 decodes FIDC [1)] |
| PA1V | PA valid | 0: Last set DD1 PA remains valid<br>1: Following DD1 PA valid |
| ID1V | DD1 SBCHID valid | 0: Last set DD1 SBCHID remains valid<br>1: Following DD1 SBCHID valid |
| PA(9..0) | Packet address | n: DD1 packet address |
| SBCHID(5..0) | Sub–channel identifier | n: DD1 sub–channel ID |

1) in this case PA and SBCHID parameters are ignored (regardless of whether PA1V/ID1V have been set or not)

### 8.1.4 Set DD2

DD configuration for transmission in packet mode

Command Settings Overview:

- Set DD2 on/off
- Set DD2 AIC on/off
- Set DD2 sub–channel ID
- Set DD2 packet address

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | $12 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| DD2E | AIC | PA2V | ID2V | 0 | | PA(9/8) | | $0X |
| PA(7..0) | | | | | | | | $XX |
| 0 | | SBCHID | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| DD2E | DD2 enable | 0: DD2 disabled<br>1: DD2 enabled |
| AIC | AIC decoding switch | 0: DD2 decodes MSC<br>1: DD2 decodes AIC [2)] |
| PA2V | DD2 PA valid | 0: Last set DD2 PA remains valid<br>1: Following DD2 PA valid |
| ID2V | DD2 SBCHID valid | 0: Last set DD2 SBCHID remains valid<br>1: Following DD2 SBCHID valid |
| PA(9..0) | Packet address | n: DD2 packet address |
| SBCHID(5..0) | Sub–channel identifier | n: DD2 sub–channel ID |

1) in this case PA and SBCHID parameters are ignored (regardless of whether PA2V/ID2V have been set or not) and the default values for AIC decoding (PA = 1023, SBCHID = 63) are used instead

### 8.1.5 Set CIF Counter and Occurrence Change

Command Settings Overview:

- Set channel decoder CIF counter
- Set channel decoder occurrence change

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | $13 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| CF | | AF | CIFCH(4..0) | | | | | $XX |
| CIFCL(7..0) | | | | | | | | $XX |
| OC(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| CF(1..0) | Change flags | 00: No change<br>01: Sub–channel organization change<br>10: Service organization change<br>11: Sub–channel & service organization change |
| AF | Alarm flag | 0: Alarm messages not accessible<br>1: Alarm messages accessible |
| CIFCH(4..0) | CIF counter (higher part) | n: CIF counter higher part (modulo 20) |
| CIFCL(7..0) | CIF counter (lower part) | n: CIF counter lower part (modulo 250) |
| OC(7..0) | Occurrence change | n: Value for CIFCL, from which the new configuration is valid |

### 8.1.6 Set Current SBCHID Long Form

Command Settings Overview:

- Set current sub–channel parameters (long form)

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | $14 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| ON | SCEFC | SBCHID | | | | | | $XX |
| SCU(9..2) | | | | | | | | $XX |
| SCU(1..0) | | EP | EPPAR | | | | CU(9..8) | $XX |
| CU(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| ON | Sub–channel on/off switch | 0: Switch sub–channel off<br>1: Switch sub–channel on |
| SCEFC | Single sub–channel for EFC | 0: Single sub–channel for EFC remains unchanged<br>1: Set SBCHID as single sub–channel for EFC |
| SBCHID(5..0) | sub–channel identifier | n: Sub–channel ID |
| SCU(9..0) | Start CU for SBCHID | n: Start CU address (0..863) |
| EP | Error Protection | 0: UEP<br>1: EEP |
| EPPAR(2..0) | Error Protection parameters | If EP = 0 (UEP):<br>000: Protection level P 1<br>001: Protection level P 2<br>010: Protection level P 3<br>011: Protection level P 4<br>100: Protection level P 5 |
| | | If EP = 1 (EEP):<br>0xx: EEP long form option 0 (protection level xx–A)<br>00: Protection level 1–A (code rate 2/8)<br>01: Protection level 2–A (code rate 3/8)<br>10: Protection level 3–A (code rate 4/8)<br>11: Protection level 4–A (code rate 6/8)<br>1xx: EEP long form option 1 (protection level xx–B)<br>00: Protection level 1–B (code rate 4/9)<br>01: Protection level 2–B (code rate 4/7)<br>10: Protection level 3–B (code rate 4/6)<br>11: Protection level 4–B (code rate 4/5) |
| CU(9..0) | Sub–channel size (number of CU's) | n: Sub–channel size in CU's (4..864) |

### 8.1.7 Set Next SBCHID Long Form

Command Settings Overview:

- Set next sub–channel parameters

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $15 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| ON | SCEFC | SBCHID | | | | | | $XX |
| SCU(9..2) | | | | | | | | $XX |
| SCU(1..0) | | EP | EPPAR | | | | CU(9..8) | $XX |
| CU(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| ON | Sub–channel on/off switch | 0: Switch sub–channel off<br>1: Switch sub–channel on |
| SCEFC | Single sub–channel for EFC | 0: Single sub–channel for EFC remains unchanged<br>1: Set SBCHID as single sub–channel for EFC |
| SBCHID(5..0) | Sub–channel identifier | n: Sub–channel ID |
| SCU(9..0) | Start CU for SBCHID | n: Start CU address (0..863) |
| EP | Error Protection | 0: UEP<br>1: EEP |
| EPPAR(2..0) | Error Protection parameters | If EP = 0 (UEP):<br>000: Protection level P 1<br>001: Protection level P 2<br>010: Protection level P 3<br>011: Protection level P 4<br>100: Protection level P 5 |
| | | If EP = 1 (EEP):<br>0xx: EEP long form option 0 (protection level xx–A)<br>00: Protection level 1–A (code rate 2/8)<br>01: Protection level 2–A (code rate 3/8)<br>10: Protection level 3–A (code rate 4/8)<br>11: Protection level 4–A (code rate 6/8)<br>1xx: EEP long form option 1 (protection level xx–B)<br>00: Protection level 1–B (code rate 4/9)<br>01: Protection level 2–B (code rate 4/7)<br>10: Protection level 3–B (code rate 4/6)<br>11: Protection level 4–B (code rate 4/5) |
| CU(9..0) | Sub–channel size (number of CU's) | n: Sub–channel size in CU's (4..864) |

### 8.1.8 Set Current SBCHID Short Form

Command Settings Overview:

- Set current sub–channel parameters (short form)

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | $16 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| ON | SCEFC | SBCHID | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| ON | Sub–channel on/off switch | 0: Switch sub–channel off<br>1: Switch sub–channel on |
| SCEFC | Single sub–channel for EFC | 0: Single sub–channel for EFC remains unchanged<br>1: Set SBCHID as single sub–channel for EFC |
| SBCHID(5..0) | Sub–channel identifier | n: Sub–channel ID |

## 8.2 'Set Configuration' Commands

### 8.2.1 Set Global Configuration

- Set channel decoder AGC values
- Set channel decoder global parameters

Command Settings Overview:

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6G |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $00 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| AGCV | 0 | dB3 | DSC | | PSC(10..8) | | | $XX |
| PSC(7..0) | | | | | | | | $XX |
| CDPV | IFM | FSYS | | SAW | ADCF | 0 | | $XX |

Command Parameters:

| Parameter | Meaning | Description | Defaults |
|---|---|---|---|
| AGCV | AGC values valid | 0: Following DSC/PSC values ignored<br>1: Following DSC/PSC values valid | |
| DSC(1..0) | Input data scale | n: Scale value | |
| PSC(10..0) | Programmable (I)FFT scale | n: Scale value | |
| CDPV | Channel decoder parameters valid | 0: Following global parameters ignored<br>1: Following global parameters valid | |
| IFM | IF input signal mode | 0: Common IF representation<br>1: Reverse IF representation | 1 |
| FSYS | Frame synchronization sensitivity level | 00: Very high<br>01: High<br>10: Low<br>11: Very low | 01 |
| SAW | SAW filter equalization switch | 0: Equalization off<br>1: Equalization on | 1 |
| ADCF | ADC format | 0: Binary ADC input format<br>1: 2's complement ADC input format | 0 |

### 8.2.2 Set TS Configuration

Command Settings Overview:

- Set TS post processing parameters

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| DAB | | | U2739M-B | | | Write | Command |

$6E

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

$21

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| DAB | | | U2739M-B | | | Write | Command |

$6C

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| PARV | COV | PKS | | ISPCnt | | | | $XX |
| TMIN | | | | | | | | $XX |
| CIRTH | | | | | | | | $XX |
| NSTH | | | | | | | | $XX |
| GFCH | | | | | | | | $XX |
| GFCL | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description | Defaults |
|---|---|---|---|
| PARV | CIR post processing parameters valid (PKS / AVG / CIRTH / NSTH / TMIN) | 0: Parameters not valid<br>1: Following parameters valid | |
| COV | CIR post processing filter coefficients valid | 0: Coefficients not valid<br>1: following coefficients valid | |
| PKS | Number of peaks required for 'CIR correct' indication | $2^n$: Required peaks | 0 |
| ISPCnt | CIR post processing average | n: CIR output average over n+1 values | 0 |
| TMIN(7..0) | CIR minimum dT output | n: Minimum dT output after CIR post processing (* 488 ns) | 0 |
| CIRTH(7..0) | CIR threshold | n.n: – Threshold value for CIR peak detection (format: 4.4 bit)<br>– Will be multiplied by ? (standard deviation) | 3.0 |
| NSTH(7..0) | Noise threshold | n: – Noise threshold value (8 bit unsigned)<br>– Will be multiplied by 32 | 0 |
| B0(15..0) | IIR filter coefficients | Coefficients for 1st order IIR filter used for CIR post processing (Q15 format required) | 0.5<br>0.5<br>0 |

### 8.2.3 Set FS Configuration

Command Settings Overview:

- Set FS post processing parameters

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | $22 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| GA | | | | | | | | $XX |
| THA | | | | | | | | $XX |
| GB | | | | | | | | $XX |
| THB | | | | | | | | $XX |
| GC | | | | | | | | $XX |
| F2FT | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description | Defaults |
|---|---|---|---|
| GA(7..0) | Area A gradient | n: Fractional part | 0.03125 |
| THA(7..0) | Area A threshold | n: Fractional part | 0.03125 |
| GB(7..0) | Area B gradient | n: Fractional part | 0.125 |
| THB(7..0) | Area B threshold | n: Fractional part | 0.25 |
| GC(7..0) | Area C gradient | n: Fractional part | 0.5 |
| F2FT(7..0) | Max. frame–to–frame tolerance | n: Maximum frequency shift in carriers (format: 3.5 bit) | 1.0 |

### 8.2.4 Set XO Configuration

Command Settings Overview:

- Set XO control parameters

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | $23 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| XO_Rough line | | | | | | | | $XX |
| XO_Fine line | | | | | | | | $XX |
| XOAVG | | | | | | 0 | | $XX |

Command Parameters:

| Parameter | Meaning | Description | Defaults |
|---|---|---|---|
| XO_B0(15..0)<br>XO_B1(15..0)<br>XO_B2(15..0)<br>XO_A1(15..0)<br>XO_A2(15..0) | IIR filter coefficients | Coefficients for 2nd order IIR filter used for XO control | 0.25<br>0.5<br>0.25<br>0<br>0 |
| XOAVG(4..0) | XO control average | n: XO control average over n+1 values | 0 |

### 8.2.5 Set HSSO / RS232 Configuration

Command Settings Overview:

- Set HSSO parameters
- Set RS232 parameters

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | $00 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| HCLK | | HCIRL | | HPAD | HDD2 | HDD1 | HCIR | $XX |
| RSBAUD | | 0 | | | | RSSEL | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| HCLK(1..0) | HSSO bit clock | 00: 0.768 MHz<br>01: 1.536 MHz<br>10: 3.072 MHz<br>11: 6.144 MHz |
| HCIRL(1..0) | HSSO CIR output length | 00: N values (DAB system mode dependent)<br>01: N/2<br>1x: N/4 |
| HPAD | HSSO PAD output switch | 0: No PAD output via HSSO<br>1: PAD output |
| HDD2 | HSSO DD2 output switch | 0: No DD2 output via HSSO<br>1: DD2 output |
| HDD1 | HSSO DD1 output switch | 0: No DD1 output via HSSO<br>1: DD1 output |
| HCIR | HSSO CIR output switch | 0: No CIR output via HSSO<br>1: CIR output |
| RSBAUD(1..0) | RS232 baud rate | 00: 19200 baud<br>01: 38400 baud<br>10: 57600 baud<br>11: 115200 baud |
| RSSEL(1..0) | RS232 output selection | 00: no output<br>01: DD1<br>10: DD2<br>11: PAD |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| UFS | USE FS module | 0: Internal set2 XTFPR module used<br>1: External USE module used |
| UFSP | USE FS post processing module | 0: Internal set2 module used<br>1: External USE module used |
| UTSP | USE TS post processing module | 0: Internal set2 module used<br>1: External USE module used |
| UXOC | USE XO control module | 0: Internal set2 module used<br>1: External USE module used |
| UDD1 | USE DD1 module | 0: Internal set2 module used<br>1: External USE module used |
| UDD2 | USE DD2 module | 0: Internal set2 module used<br>1: External USE module used |
| UPAD | USE PAD extraction module | 0: Internal set2 module used<br>1: External USE module used |
| UTII | USE TII module | 0: Internal set2 module used<br>1: External USE module used |
| UAMD ... UNMI | Reserved | |

### 8.2.6 Set WAGC Configuration

Command Settings Overview:

- Set WAGC rising edge / falling edge parameters

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $26 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write | Command | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| WRISE(3..0) | | | | WS | 0 | | WV | $XX |
| WRISE(11..4) | | | | | | | | $XX |
| WFALL(1..0) | | WRISE(17..12) | | | | | | $XX |
| WFALL(9..2) | | | | | | | | $XX |
| WFALL(17..10) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| WV | WAGC values valid | 0: use default WAGC values<br>1: use following WAGC values |
| WRISE(17..0) | WAGC rising edge time marker | n: value for WAGC rising edge |
| WFALL(17..0) | WAGC falling edge time marker | n: value for WAGC falling edge |

### 8.2.7 Set RCC Slot Configuration

Command Settings Overview:

- Set RCC slot data

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6E |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | $27 |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | |
| DAB | | | U2739M-B | | | Write Command | | $6C |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| RCC(7..0) | | | | | | | | $XX |
| RCC(15..8) | | | | | | | | $XX |
| RCC(23..16) | | | | | | | | $XX |
| RCC(31..24) | | | | | | | | $XX |
| RCC(39..32) | | | | | | | | $XX |
| RCC(47..40) | | | | | | | | $XX |
| RCC(55..48) | | | | | | | | $XX |
| RCC(63..56) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| RCC(63..0) | RCC slot data | |

### 8.2.8 Set RFU

Command Settings Overview:

- Set RFU parameters

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| DAB | | | U2739M-B | | | Write | Command |

$6E

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

$30

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| DAB | | | U2739M-B | | | Write | Command |

$6C

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| (reserved) | | | | | | | | $XX |
| (reserved) | | | | | | | | $XX |
| (reserved) | | | | | | | | $XX |
| (reserved) | | | | | | | | $XX |
| RFU4 | | | | | | | | $XX |
| RFU5 | | | | | | | | $XX |
| RFU6 | | | | | | | | $XX |
| ... | | | | | | | | $XX |
| ... | | | | | | | | $XX |
| RFU42 | | | | | | | | $XX |
| RFU43 | | | | | | | | $XX |
| RFU44 | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| (reserved) | | Reserved for internal use (Atmel Wireless & Microcontrollers will deliver default values, if necessary) |
| RFU4..44 | | Reserved for future use |

## 8.3 ’Read Status’ Commands

### 8.3.1 Read Global Status

Command Overview:

- Get DAB system mode
- Get OAK core operating mode
- Get synchronization status
- Get AGC information

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

$6F

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

$40

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

$6D

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| DABMODE | | OAKMODE | | MV | FSLI | SLI | WDSP | $XX |
| 0 | | | CIRS | CCIR | | CAFC | | $XX |
| 0 | PSLI | | | | IDSL | | P(8) | $XX |
| P(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| DABMODE(1..0) | DAB system mode | 00: DAB system mode 4<br>01: DAB system mode 1<br>10: DAB system mode 2<br>11: DAB system mode 3 |
| OAKMODE(1..0) | OAK operating mode | 00: Normal stand–alone<br>01: USE boot mode<br>10: XUSE boot mode<br>11: HOST boot mode |
| MV | MODE_VALID line status | |
| FSLI | FSLI line status | |
| SLI | SLI line status | |
| CIRS | CIR status | 0: No CIR detected<br>1: CIR correct |
| CCIR(1..0) | Coded CIR status | 00: \|average\| ? N/64<br>01: N/64 < \|average\| ? N/8<br>10: \|average\| > N/4<br>11: rfu. |
| CAFC(1..0) | Coded AFC status | 00: $\|dF_{FRAME}\|$ ? TA<br>01: TA < $\|dF_{FRAME}\|$ ? TB<br>10: TB < $\|dF_{FRAME}\|$ < 16 kHz<br>11: $\|dF_{FRAME}\|$ ? 16 kHz |
| PSLI(3..0) | Precise signal level information | 0000: Very weak signal<br>...<br>1111: Very strong signal |
| IDSL(1..0) | Input data signal level | 00: Weak input signal<br>01: Typical input signal<br>10: Strong input signal<br>11: rfu. |
| P(8..0) | Calculated in–band power | |
| WDSP | Watchdog DSP | Toggels every 24 ms from 0 to 1 |

### 8.3.2 Read Synchronization Status

Command Overview:

- Get TS control value
- Get FS control value

| Address Mode | | | | | | | | Command sequence: |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | $41 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| DT(9..2) | | | | | | | | $XX |
| DT(1..0) | | 0 | | DF(19..16) | | | | $XX |
| DF(15..8) | | | | | | | | $XX |
| DF(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| DT(9..0) | Detected time deviation | n: Cycle count (signed, @2.048 MHz) 1) |
| DF(19..0) | Detected channel frequency deviation | n: Deviation in carriers (signed, Q11 format) |

1) Signed values refers to virtual zero at $T_{guard}/2$

### 8.3.3 Read CIR Status

Command Overview:

- Get CIR post processing results [1)]

| | Command sequence: |
|---|---|
| **Address Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 1 0 1 1 1 1 | |
| DAB / U2739M-B / Write Command | $6F |
| **Data Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 0 0 0 0 1 0 | $42 |
| **Address Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 1 0 1 1 0 1 | |
| DAB / U2739M-B / Write Command | $6D |
| **Data Mode** | |
| **7 6 5 4 3 2 1 0** | |
| P_FIRST(15..8) | $XX |
| P_FIRST(7..0) | $XX |
| P_AGV(15..8) | $XX |
| P_AGV(7..0) | $XX |
| P_LAST(15..8) | $XX |
| P_LAST(7..0) | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| P_FIRST(15..0) | Index of 1st CIR peak above CIR threshold | n: Cycle count (signed, @2.048 MHz) [2)] |
| P_AVG(15..0) | Index of CIR average value | n: Cycle count (signed, @2.048 MHz) |
| P_LAST(15..0) | Index of last CIR peak above CIR threshold | n: Cycle count (signed, @2.048 MHz) |

1) If time synchronization has lost all values are set to $8000 !
2) Signed values refers to zero at $T_{guard}/2$

## 8.4 ’Read Data’ Commands

### 8.4.1 Read ASD Header Data

Command Overview:

- Get MPEG audio header

| | | | | | | | | **Command sequence:** |
|---|---|---|---|---|---|---|---|---|
| **Address Mode** | | | | | | | | |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6F |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Data Mode** | | | | | | | | |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | $50 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Address Mode** | | | | | | | | |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6D |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Data Mode** | | | | | | | | |
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| MPG_HW1(15..8) | | | | | | | | $XX |
| MPG_HW1(7..0) | | | | | | | | $XX |
| MPG_HW2(15..8) | | | | | | | | $XX |
| MPG_HW2(7..0) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| MPG_HW1(15..0) | 1st MPEG header word | Sync. word ($FFFx) expected |
| MPG_HW2(15..0) | 2nd MPEG header word | MPEG stream signature |

### 8.4.2 Read X–PAD

Command Overview:

- Get MPEG ancillary data (X–PAD)

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 0 | 1 | 0 | XPNUM | | | $5X |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| X–PAD0 | | | | | | | | $XX |
| ... | | | | | | | | |
| X–PAD31 | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| XPNUM | X–PAD block number n (n from 1..5) | The maximum X–PAD capacity supported by the U2739M-B is 64kbit/s. The access is splitted into 6 blocks (numbered 1..5) of 32 bytes. The blocks are time aligned, that means block 1 is the first block in an MPEG frame after audio samples. |
| X–PADm | X–PAD byte m | Byte 0 is the first byte of block n, byte 31 the last one. It is followed by the first one of block n+1. |
| | Read RFU | Use MC command “RFU” to read block 6 |

### 8.4.3 Read F–PAD

Command Overview:

- Get MPEG ancillary data (F–PAD)

| | Command sequence: |
|---|---|
| **Address Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 1 0 1 1 1 1 | |
| DAB U2739M-B Write Command | $6F |
| **Data Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 0 1 1 0 0 0 | $58 |
| **Address Mode** | |
| **7 6 5 4 3 2 1 0** | |
| 0 1 1 0 1 1 0 1 | |
| DAB U2739M-B Write Command | $6D |
| **Data Mode** | |
| **7 6 5 4 3 2 1 0** | |
| F–PAD0 | $XX |
| F–PAD1 | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| F–PAD0 | F–PAD byte 0 | |
| F–PAD1 | F–PAD byte 1 | |

### 8.4.4 Read AIC Data

Command Overview:

- Get AIC data

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | AICNUM | | | | $6X |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| AIC0 | | | | | | | | $XX |
| ... | | | | | | | | |
| AIC31 | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| AICNUM | AIC block number n | The maximum AIC capacity is 512 bytes.<br>The access is splitted into 16 blocks (numbered 0..15) of 32 bytes.<br>The blocks are time aligned, that means block 0 is the first filled block. |
| AICm | AIC byte m | Byte 0 is the first byte of block n, byte 31 the last one. It is followed by the first one of block n+1. |

### 8.4.5 Read TII Data

Command Overview:

- Get TII data

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 1 | 0 | 0 | TIINUM | | $7X |

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| TII0 | | | | | | | | $XX |
| ... | | | | | | | | |
| TII31 | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| TIINUM | TII block number n | The maximum TII capacity is 128 bytes.<br>The access is splitted into 4 blocks (numbered 0..3) of 32 bytes.<br>The blocks are time aligned, that means block 0 is the first filled block. |
| TIIm | TII byte m | Byte 0 is the first byte of block n, byte 31 the last one. It is followed by the first one of block n+1. |

### 8.4.6 Read EFC Data

Command Overview:

- Get EFC data

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 1 | 0 | 0 | 0 | 0 | 0 | EFCSEL | | $8X |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write Command | | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| EFC(7..0) | | | | | | | | $XX |
| EFC(15..8) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| EFCSEL | EFC selection | 00: EFC of FIC<br>01: EFC of all MSC applications |
| EFC(15..0) | EFC value for chosen application | n: EFC value summarized over...<br>... 12 FIB's (DAB mode 1)<br>... 3 FIB's (DAB mode 2)<br>... 4 FIB's (DAB mode 3)<br>... 6 FIB's (DAB mode 4) |

### 8.4.7 Read FIC Data

Command Overview:

- Get FIB bytes

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

\$6F

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 1 | 0 | 0 | 1 | FIBNUM | | | |

\$9X

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

\$6D

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| FIB0 | | | | | | | |
| ... | | | | | | | |
| FIB31 | | | | | | | |

\$XX

\$XX

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| FIBNUM | FIB number n | Possible FIB numbers DAB mode dependent:<br>0..11 (DAB mode 1)<br>0..2 (DAB mode 2)<br>0..3 (DAB mode 3)<br>0..5 (DAB mode 4) |
| FIBm | FIB byte m | Each FIB consists of 32 bytes. The order of the FIB bytes and bits corresponds to the serial FIC processing. That means:<br>(1) Byte order:<br>The first 8 output bits after FIC processing represent FIB byte 0 of FIB number 0, the next ones FIB byte 1 of FIB number 0 and so on.<br>(2) Bit order:<br>The FIB bytes are given out MSB first. The first outgoing bit represents bit 7 of the corresponding byte, the next one bit 6 and so on. The FIB bits are numbered from bit 0 (MSB of FIB0) up to bit 255 (LSB of FIB31).<br>NOTE:<br>The last 2 bytes of an FIB represent the result of the U2739M internal CRC check. That means, if these bytes are \$00 both, the internal CRC check was successful and the FIB data bytes are correct. |

### 8.4.8 Read RCC Slot

Command Overview:

- Get RCC slot data

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $A0 |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| RCC(7..0) | | | | | | | | $XX |
| RCC(15..8) | | | | | | | | $XX |
| RCC(23..16) | | | | | | | | $XX |
| RCC(31..24) | | | | | | | | $XX |
| RCC(39..32) | | | | | | | | $XX |
| RCC(47..40) | | | | | | | | $XX |
| RCC(55..48) | | | | | | | | $XX |
| RCC(3..56) | | | | | | | | $XX |

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| RCC(63..0) | RCC slot data | |

### 8.4.9 Read Slot Pointer

Command Overview:

- Get RCC RX/TX slot pointer

**Command sequence:**

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

$6F

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

$A1

| Address Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| DAB | | | U2739M-B | | | Write Command | |

$6D

| Data Mode | | | | | | | |
|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| TXPTR | | | | RXPTR | | | |

$XX

Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| RXPTR(3..0) | RCC RX slot pointer | |
| TXPTR(3..0) | RCC TX slot pointer | |

### 8.4.10 Read RFU

Command Overview:

- Get RFU data

**Command sequence:**

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6F |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | $9X |

| Address Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| DAB | | | U2739M-B | | | Write | Command | $6D |

| Data Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | |
| RFU0 | | | | | | | | $XX |
| ... | | | | | | | | |
| RFU43 | | | | | | | | $XX |

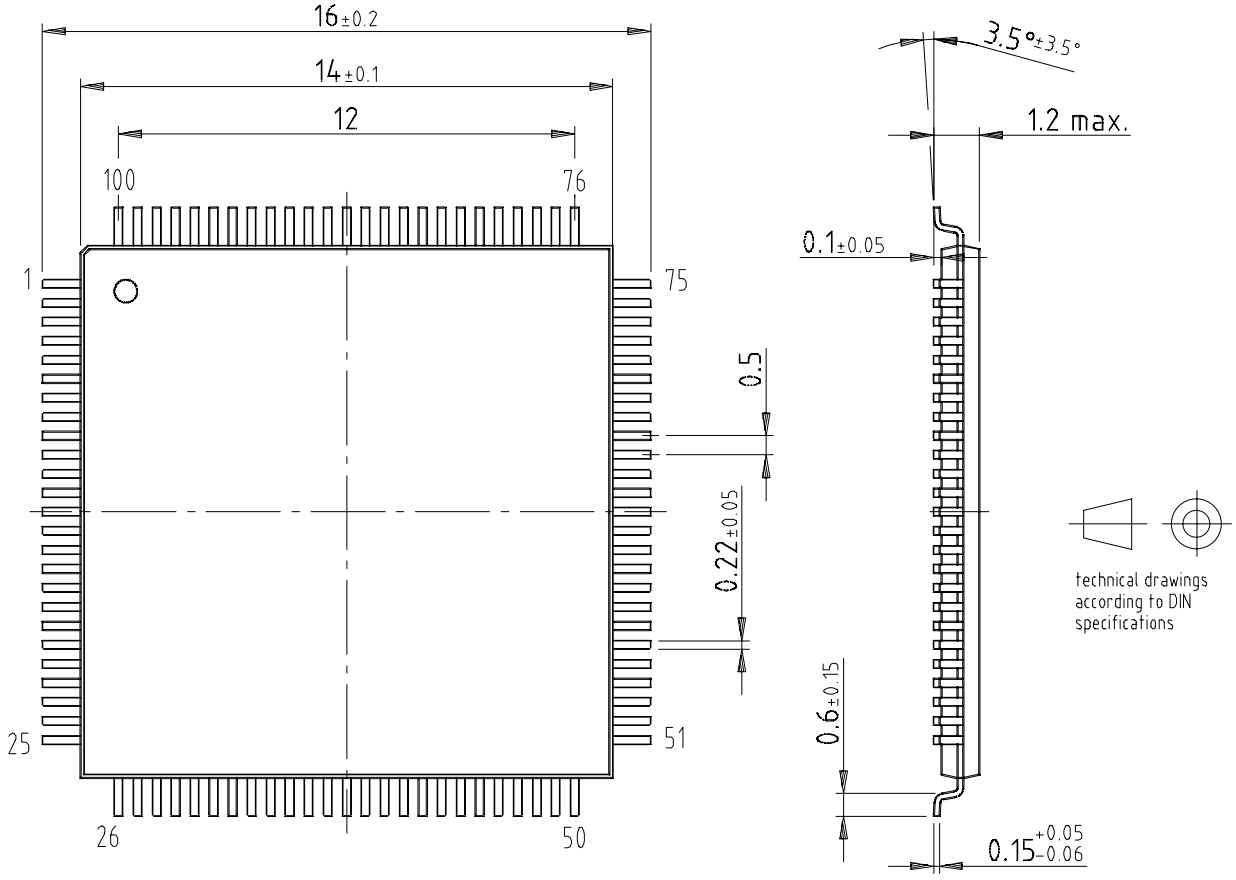
Command Parameters:

| Parameter | Meaning | Description |
|---|---|---|
| XPAD0..31 | XPAD block 6 | See: read XPAD command |
| RFU0..11 | | Reserved for future use |

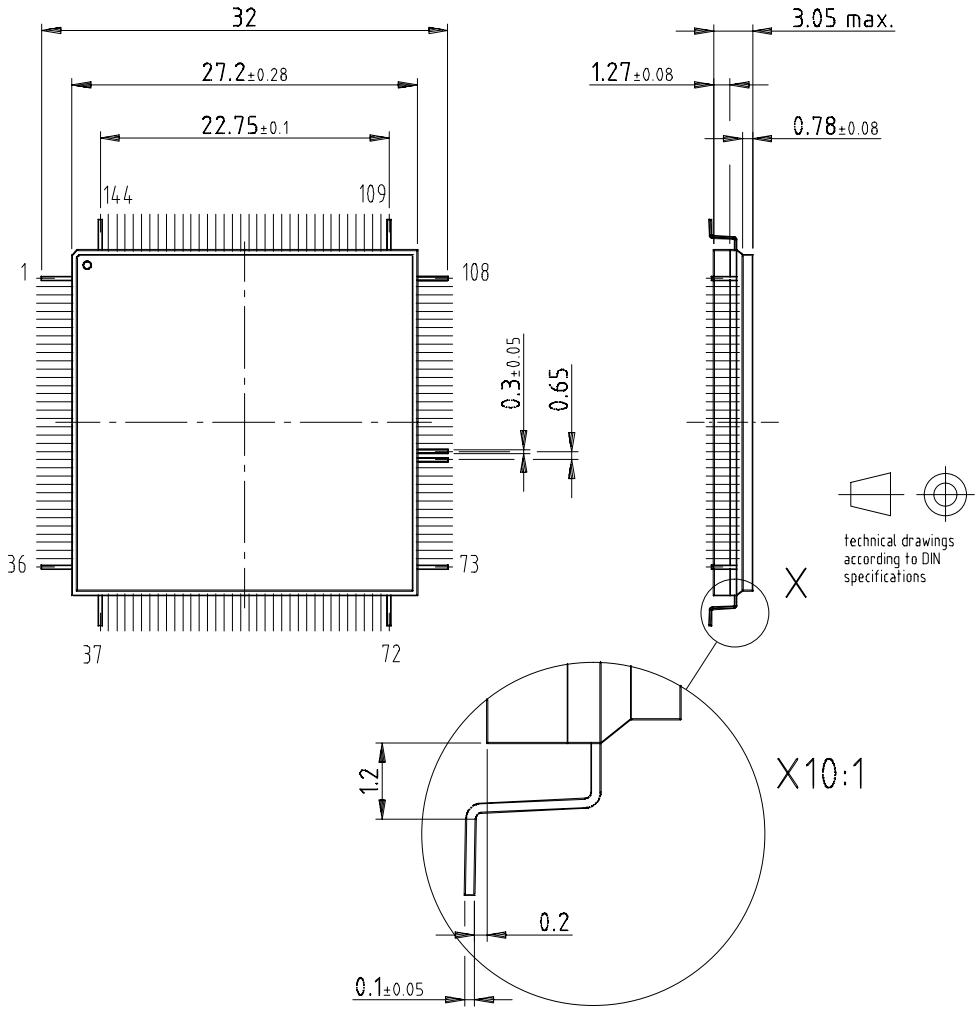
# 9 Package Information

Package: T-PQFP-G 100
(acc. JEDEC OUTLINE No. MS-026)

Dimensions in mm



Package: CQFP- 144
Dimensions in mm



## Ozone Depleting Substances Policy Statement

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2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Atmel Germany GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

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